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AT&T
Guilford Center
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Greensboro, NC 27420

SARGIC HFET DESIGN MANUAL

June 2, 1988

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SARGIC HFET DESIGN MANUAL

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DIGITAL CIRCUIT DESIGN WITH SARGIC/HFET PROCESS

INTRODUCTION:

This manual describes the design and layout of GaAs integrated circuits using the SARGIC/HFET (Self Aligned Refractory Gate Integrated Circuit/Hetro-junction FET) process. It is divided into three sections, layout design rules, device terminal characteristics, and process control monitor (PCM).

The first section outlines the layout of digital GaAs circuits in the SARGIC/HFET, 2 μ m design rules. It describes the circuit layout procedure level by level, and includes the process's layout design rules.

The second section contains the terminal characteristics of Enhancement (EHFET), Depletion (DHFET), and diode devices. This includes drain and gate I/V and capacitance curves modeled by AT&T's ADVICE circuit simulator at 25 and 125°C.

The last section includes the design and layout of the Process Control Monitor (PCM). The PCM contains test structures for process control and the extraction of circuit simulator models and device S parameters. This allows the foundry to test for process biases, extract process/device parameters, ADVICE models, and gate propagation delays and noise margins.

*Gallium
Arsenide*

AsGa
↑

FOUNDY OPERATION:

AT&T prefers to receive a customer's design on a magnetic tape using GDS II format. AT&T foundry mask sets have requirements that may not be met by a customer generated reticle mask. Also the proper stepper alignment features must be incorporated on the reticle mask with the primary die and Process Control Monitors.

DIGITAL SARGIC HFET PROCESS

The AT&T DIGITAL SARGIC HFET process is based on $1\mu\text{m}$ gate length Enhancement (EHFET) and Depletion (DHFET) devices. It is a self-aligned semi-planar process that implements two levels of metal interconnect with $2\mu\text{m}$ line widths and spacing. The two metal layers are separated by an oxynitride dielectric.

The process can fabricate EHFETs, DHFETs, schottky diodes, N^+ implanted resistors, and MIM (Metal Insulator Metal) capacitors. Device isolation is achieved by oxygen implant between active regions, which yields a semi-planar process.

The process gives the freedom to layout active and passive component circuits with a full two level metal interconnect. However, designers should adhere to the following guidelines when laying out a circuit:

Metal runners are not allowed to cross an HFET gate. Metal crossing over a gate can induce piezo-electric effects that cause shifts in device threshold voltages.

No metal except gate tabs and ohmic contacts is to be in contact with the substrate. This rule forbids the use of gate and ohmic metals for the purpose of interconnects in radiation hardened circuits.

It is recommended that top metal is used for power rails, due to the lower sheet resistance and higher current carrying density. The rails should be made as wide as possible to prevent rail collapsing during exposure to radiation, as well as, designing for electro-migration limits.

Non-radiation hardened circuits can use gate and ohmic metals for interconnect. However, the runners should be kept as short as possible due to their higher sheet resistance.

Be certain that all HFET gates are laid out in the same direction. The process does not allow multiple gate orientations in order to eliminate threshold voltage shifts due to piezo-electric effects.

It is recommended that HFETs in excess of $50\mu\text{m}$ wide be broken into multiple fingers if possible and drive the gates from both ends. This alleviates the high gate RC constant associated with tungsten silicide gates.

All schottky diodes should be made in EHFET tubs. Diodes made on the DHFET surface are not repeatable and should not be used.

The SARGIC HFET process allows a minimum of $100 \times 100\mu\text{m}$ bond pads with $25\mu\text{m}$ spacing. However, designers should make sure that probe cards can be made to accommodate the design. If probe cards cannot be made for the above design rules, then the pads can be made $120 \times 120\mu\text{m}$ with $80\mu\text{m}$ spacing for which probe cards are readily available.

FUTURE UPDATES

The SARGIC/HFET process design manual will be updated in the future to keep abreast of the latest developments in modeling, process, and design support. Future updates will include, but not limited to, the following information:

- Reduction in layout design rules for the advanced technology program.
- Improved data fitted device terminal characteristics in ADVICE circuit simulator terminal characteristics and model parameters for temperatures below 25 and above 125°C.
- Improvements and updates on the Process Control Monitors.
- Improvement in design support.

This manual is written for the designers of GaAs IC's in AT&T's SARGIC/HFET process. Input from all designers is welcome for adding further information or improvement to the manual.

SARGIC HFET PROCESS DESIGN RULES

LIST OF FIGURES AND TABLES

- Figure 1. Alignment Marks
- Figure 2. EHFET Tub
- Figure 3. Implant Isolation
- Figure 4. HFET Gate Formation
- Figure 5. N+ Implant
- Figure 6. Ohmic Metal Contact
- Figure 7. Dielectric VIA1
- Figure 8. Bottom Metal
- Figure 9. Dielectric VIA2
- Figure 10. Top Metal
- Figure 11. Passivation
- Figure 12. Device Geometry Design Rules
- Figure 13. Device and Gate Spacing Design Rules
- Figure 14. EHFET Tub Design Rules
- Figure 15. EHFET Tub Diode Design Rules
- Figure 16. VIA and Interconnect Design Rules
- Figure 17. TOPMET/BOTMENT VIA and Interconnect Design Rules
- Figure 18. Capacitor Design Rules
- Figure 19. N+ Implanted Resistor Design Rules
- Figure 20. Bonding Pad Design Rules
- Tables 1-2. Process Parameter Specifications
- Table 3. Device Breakdown Voltages
- Table 4. Processed and Non-Processed Mask Levels
- Table 5. Design Rule Summary

PROCESS FLOW:

1. ALIGNMENT MARKS:

MASK TONE: CLEAR ON OPAQUE

The first mask is the stepper alignment features which are transferred onto the substrate. This level is the alignment reference for several mask levels. The alignment marks are placed in the dicing lanes by AT&T.

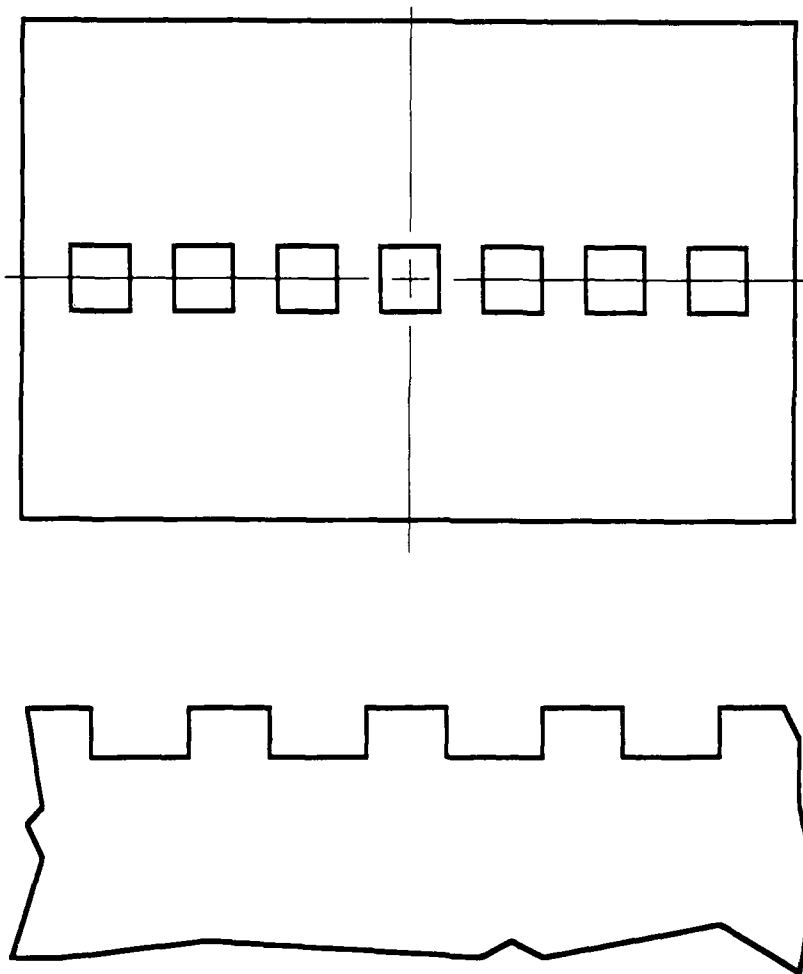


FIGURE 1

2. EHFET TUB (ETB):

MASK TONE: CLEAR ON OPAQUE

The SARGIC process starts with an all DHFET substrate. The formation of an EHFET requires the etching of the first two top layers in the starting substrate to form an EHFET TUB. This tub is about 500 angstroms deep.

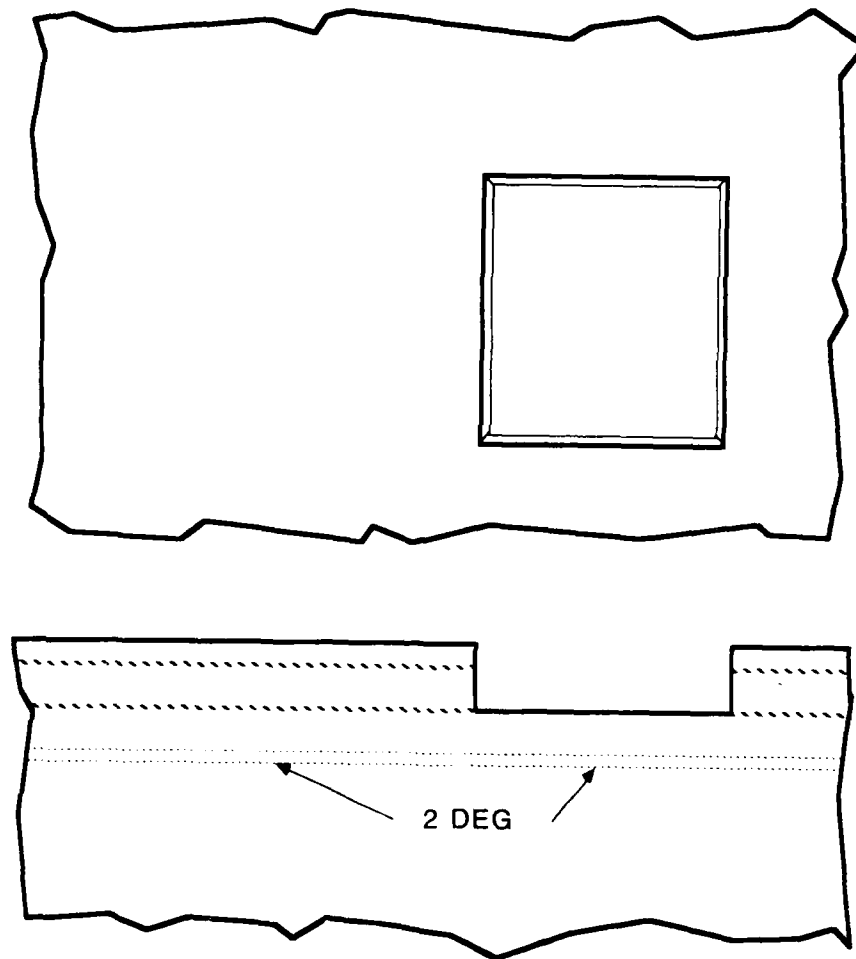


FIGURE 2

3. IMPLANT ISOLATION (ISO):

MASK TONE: OPAQUE ON CLEAR

Device isolation is achieved by an oxygen implant into the substrate. This level will determine the active device dimensions.

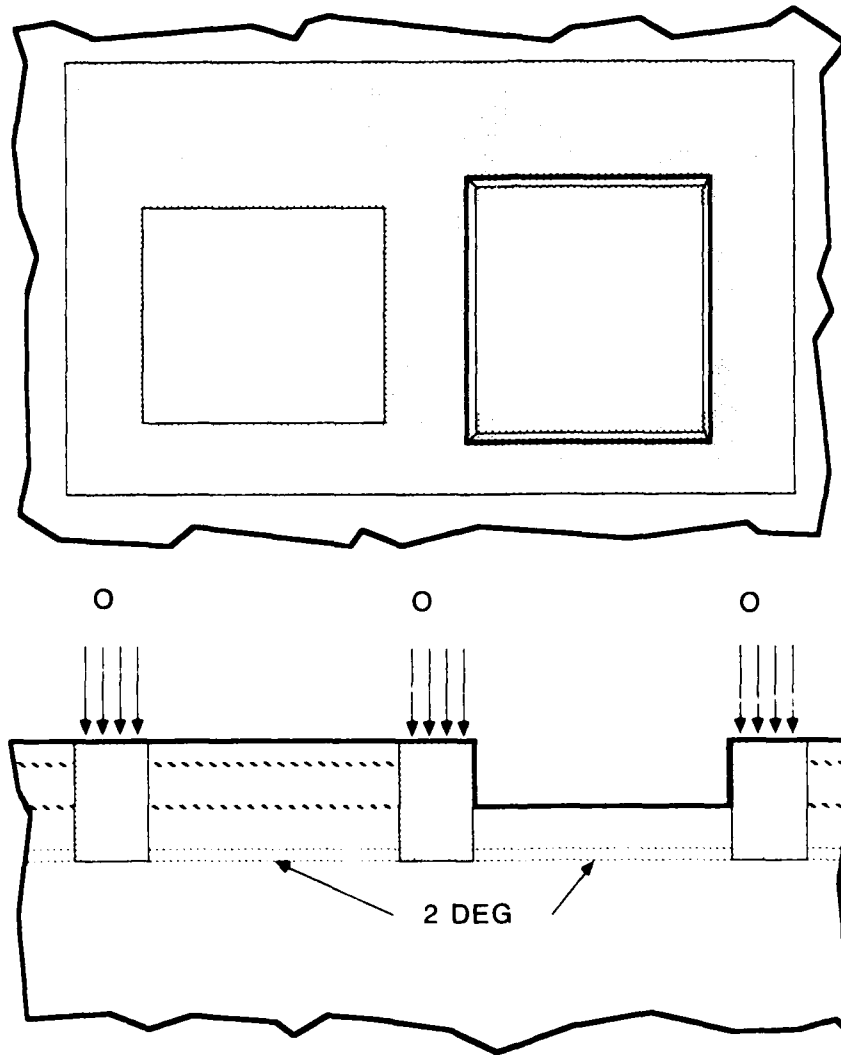


FIGURE 3

4. EHFET/DHFET GATE FORMATION (GMT):

MASK TONE: OPAQUE ON CLEAR

The rectifying FET gates and schottky diodes are formed by a WSix metal. The gate metal must be compensated by $+0.25\mu\text{m}$ to offset process biases. This will result in a final $1\mu\text{m}$ gate lengths. Schottky diode contacts need not be compensated. This metal should not be used for interconnect especially in radiation hardened circuits.

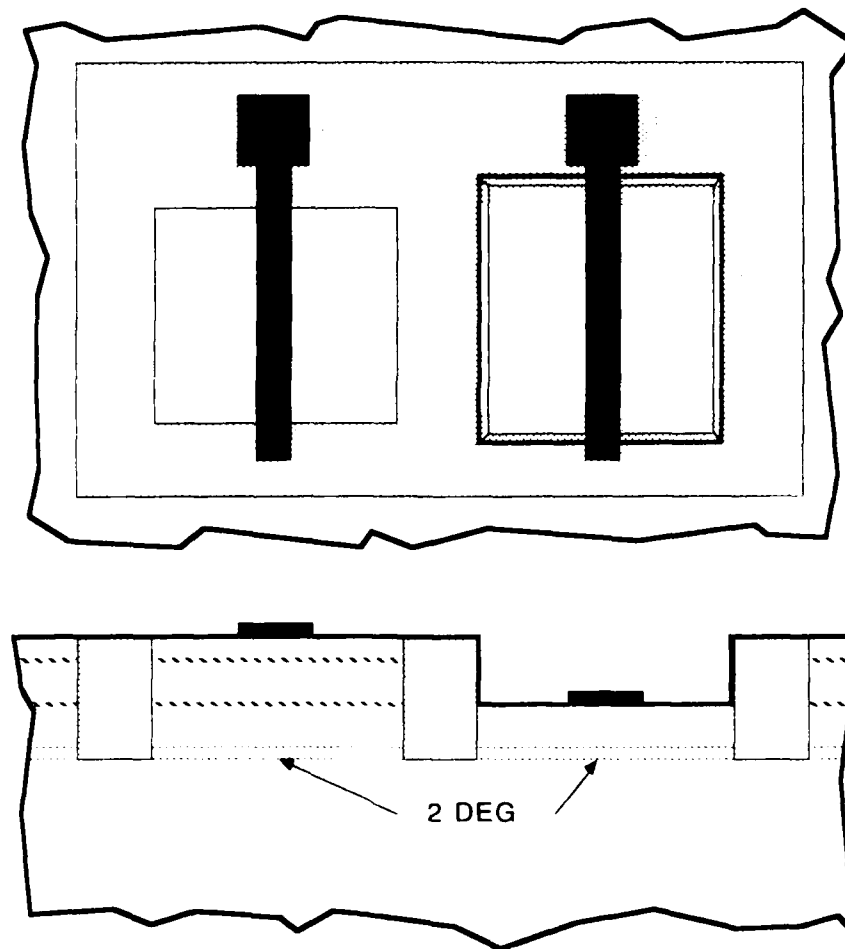


FIGURE 4

5. N+ IMPLANT (NIP):

MASK TONE: CLEAR ON OPAQUE

The N+ implant mask is used for forming the drain and source contact regions. It is also used to form the implanted resistors and schottky diode cathodes. N+ runners for interconnect should not be used for radiation hardened circuits.

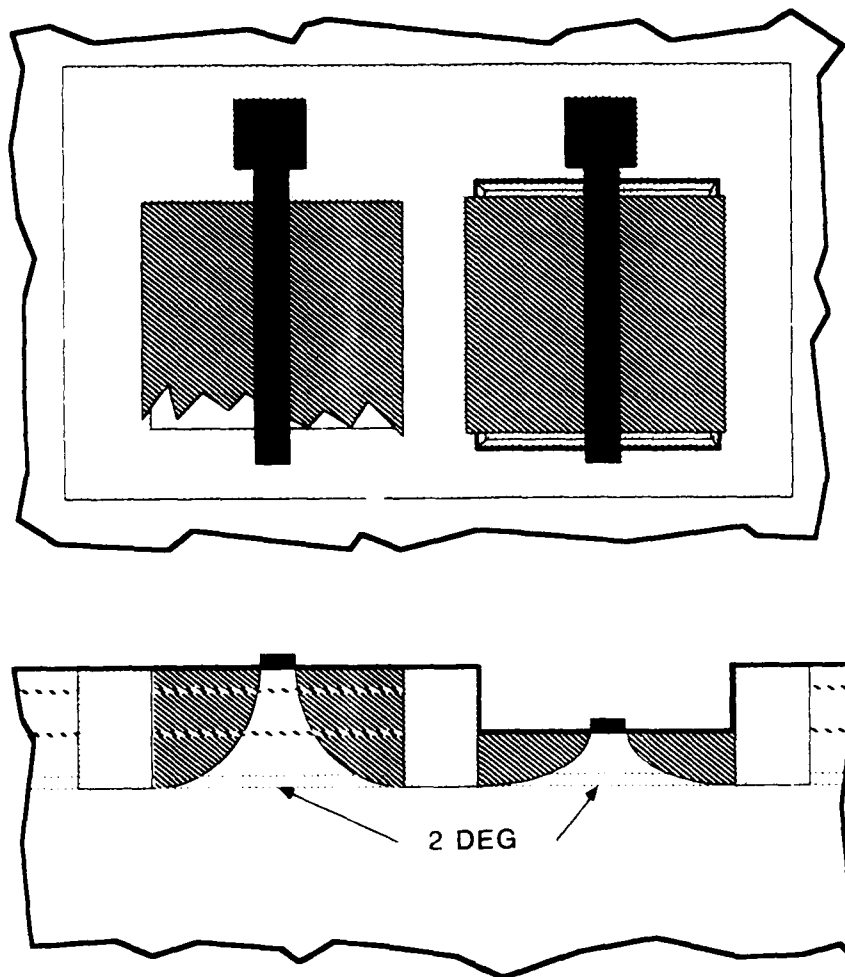


FIGURE 5

6. OHMIC METAL CONTACT (OMT):

MASK TONE: CLEAR ON OPAQUE

Ohmic metal is defined on top of the N+ implant and alloyed to form the ohmic contact. This metal should not be used for interconnect especially for radiation hardened circuits.

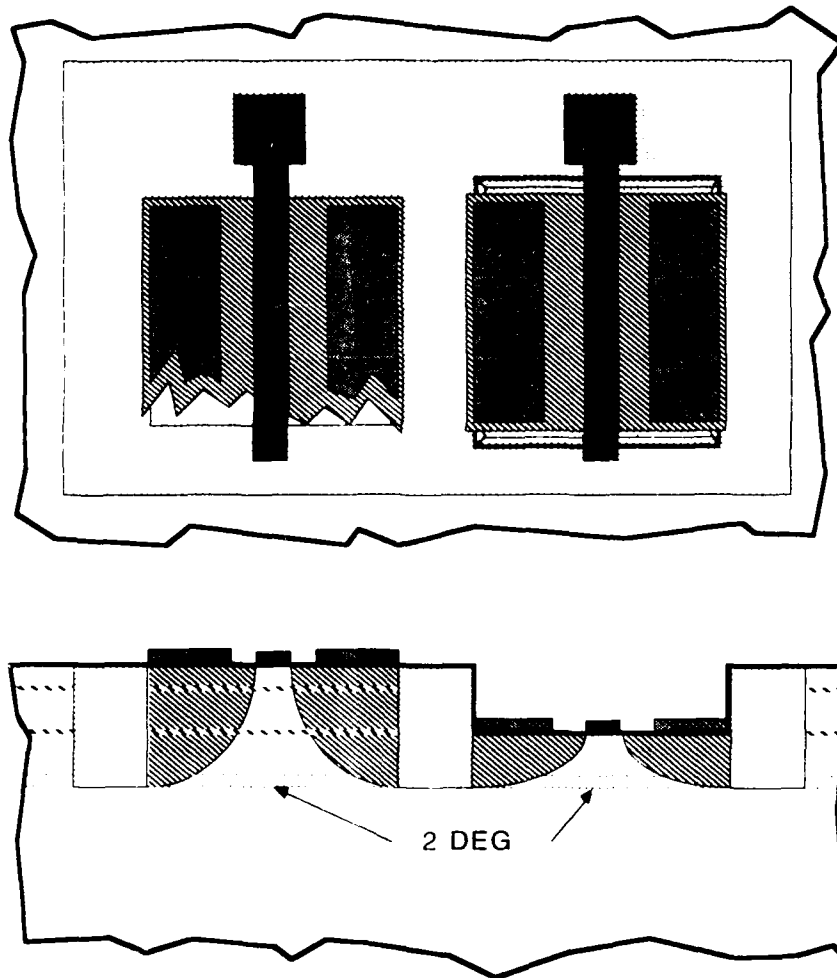


FIGURE 6

7. DIELECTRIC VIA ONE (VIA1):

A layer of oxynitride is deposited on top of the gate and ohmic metals. A via is etched wherever an electrical contact is desired to the gate tab or ohmic metal.

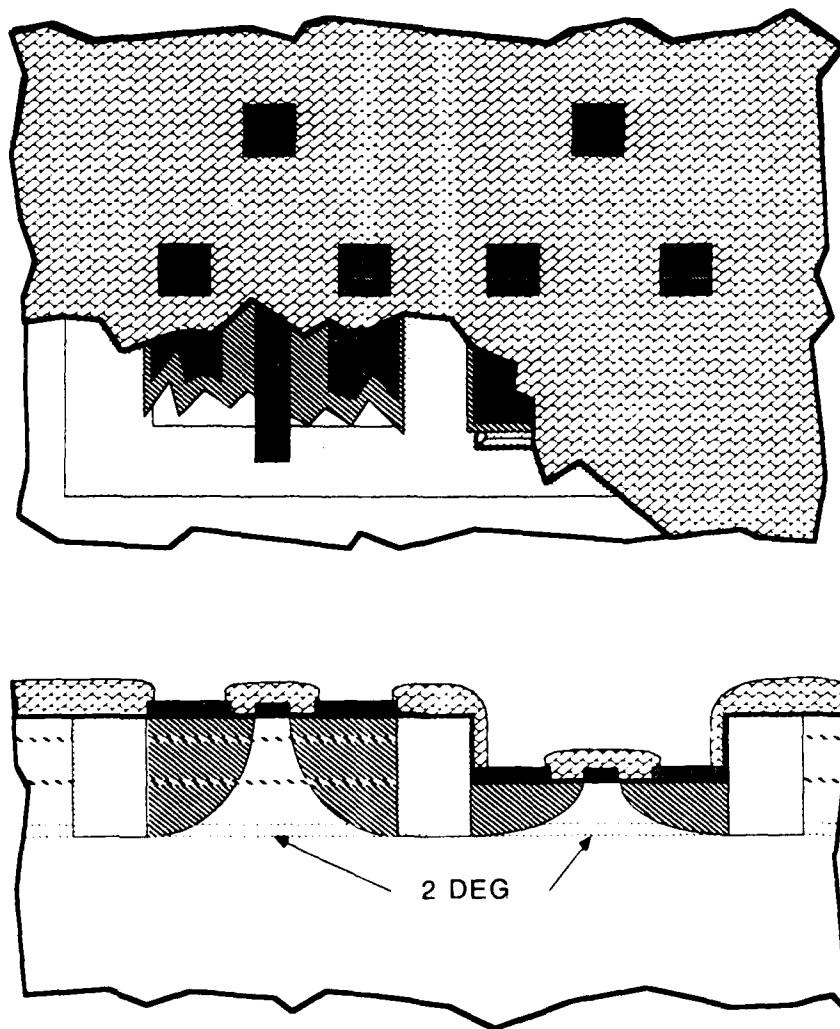


FIGURE 7

8. BOTTOM METAL (BOTMET, BMT):

MASK TONE: CLEAR ON OPAQUE

BOTMET is the first metal interconnection level. All electrical contacts to gate and ohmic metal must be done with BOTMET using VIA 1. This level also forms the bottom electrode of MIM capacitors and a bottom bonding pad. BOTMET must be compensated by $-0.125\mu\text{m}$ to offset process biases.

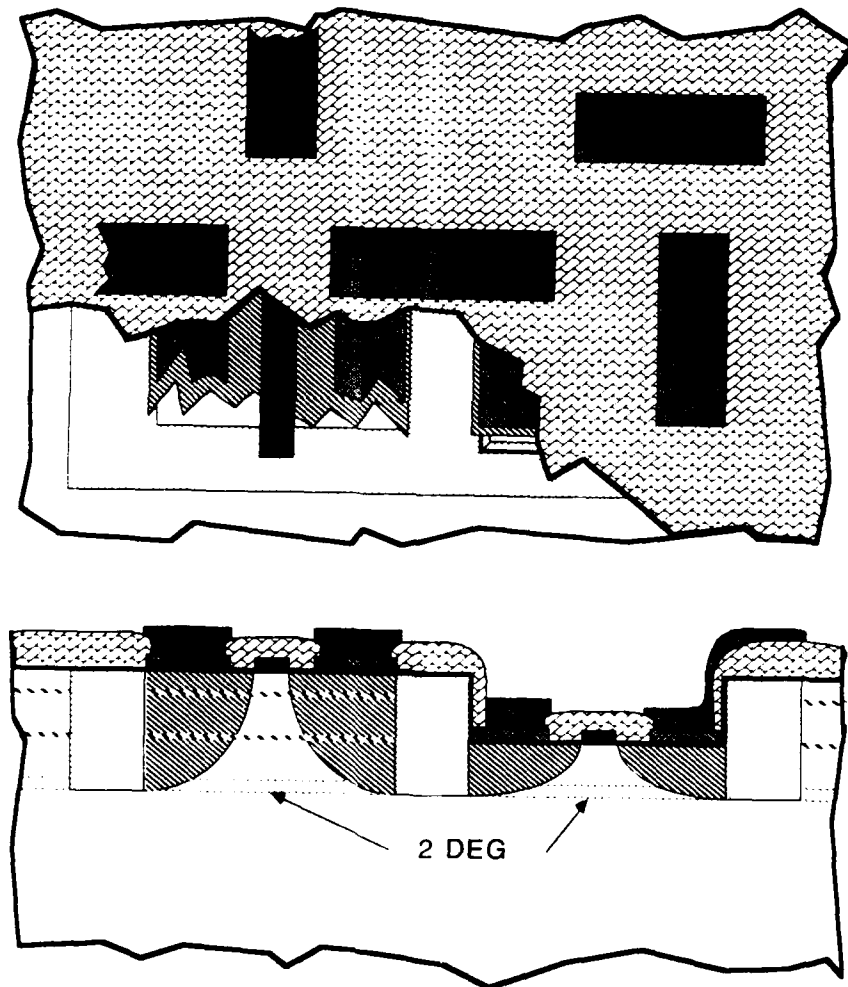


FIGURE 8

9. DIELECTRIC VIA 2 (VIA2):

MASK TONE: CLEAR ON OPAQUE

Subsequent to BOTMET a second layer of oxynitride is deposited to isolate the two metal layers. A via will be etched wherever an electrical contact is desired between top metal and bottom metal.

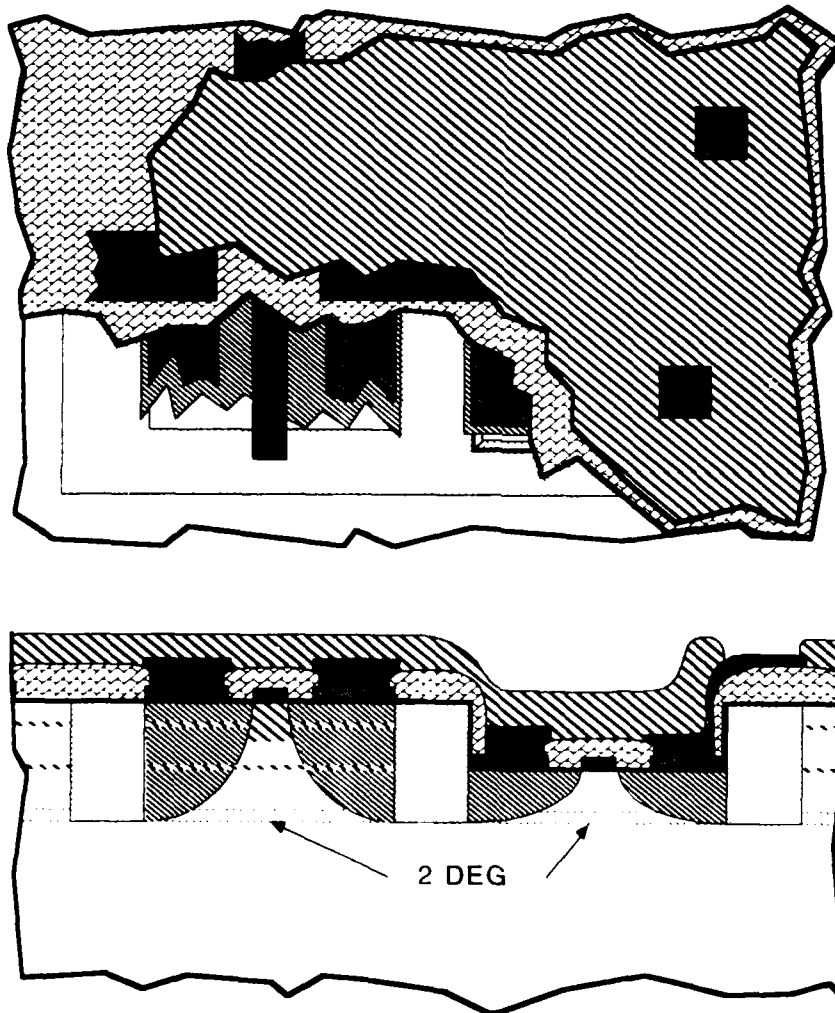


FIGURE 9

10. TOP METAL (TOPMET, TMT):

MASK TONE: CLEAR ON OPAQUE

TOPMET is the second interconnection level that links BOTMET to BOTMET using VIA 2. This level serves as the top electrode of MIM capacitors and top bonding pad. TOPMET must be compensated by $-0.125\mu\text{m}$ to offset process biases.

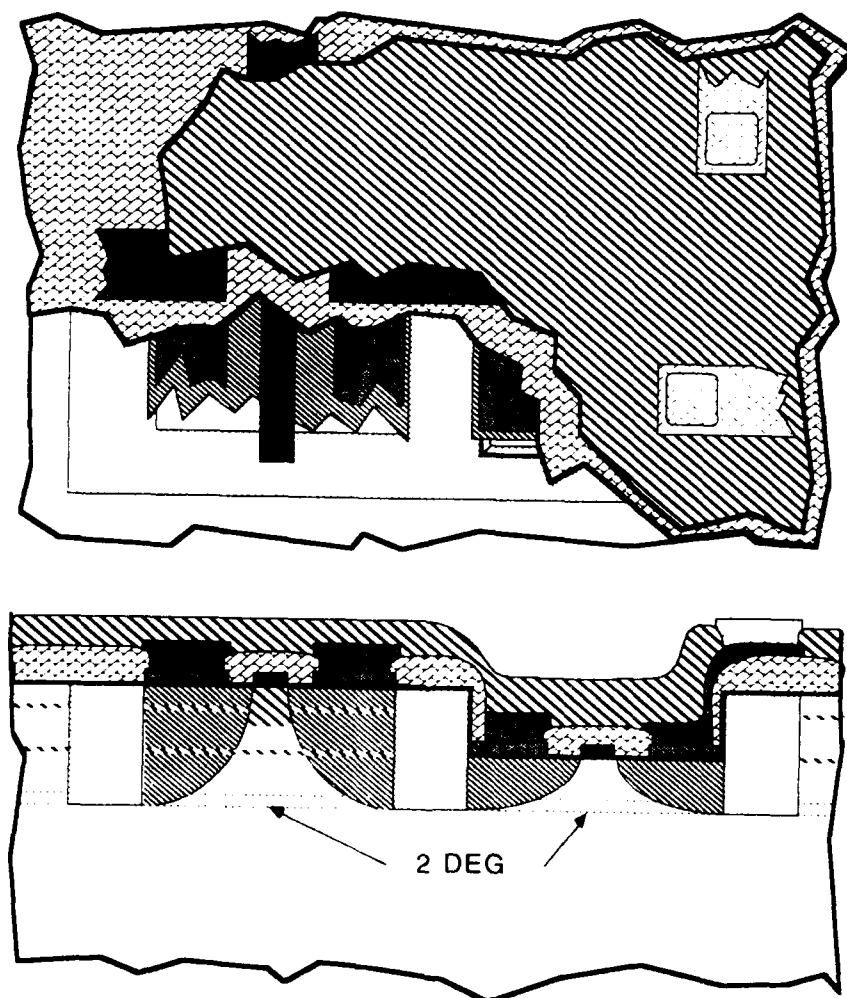


FIGURE 10

11. PASSIVATION (PAS):

MASK TONE: CLEAR ON OPAQUE

Subsequent to TOPMET a passivating layer of oxynitride is deposited to protect the circuit. This level will have openings for the bond pad wires.

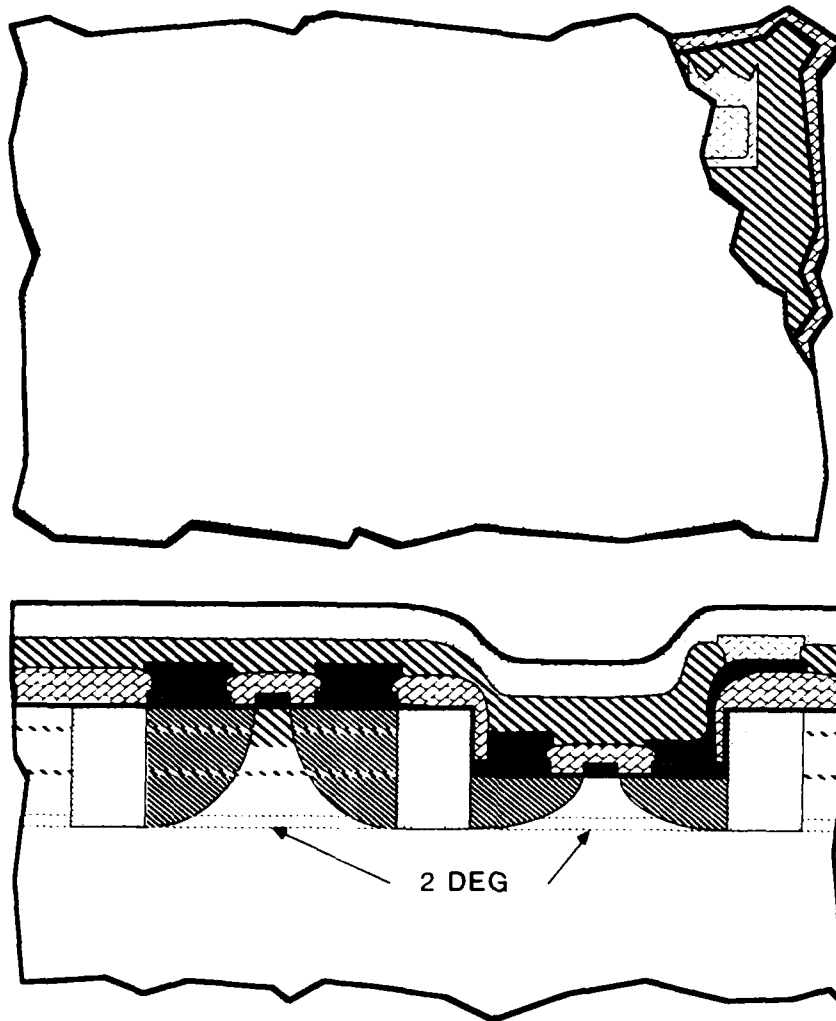
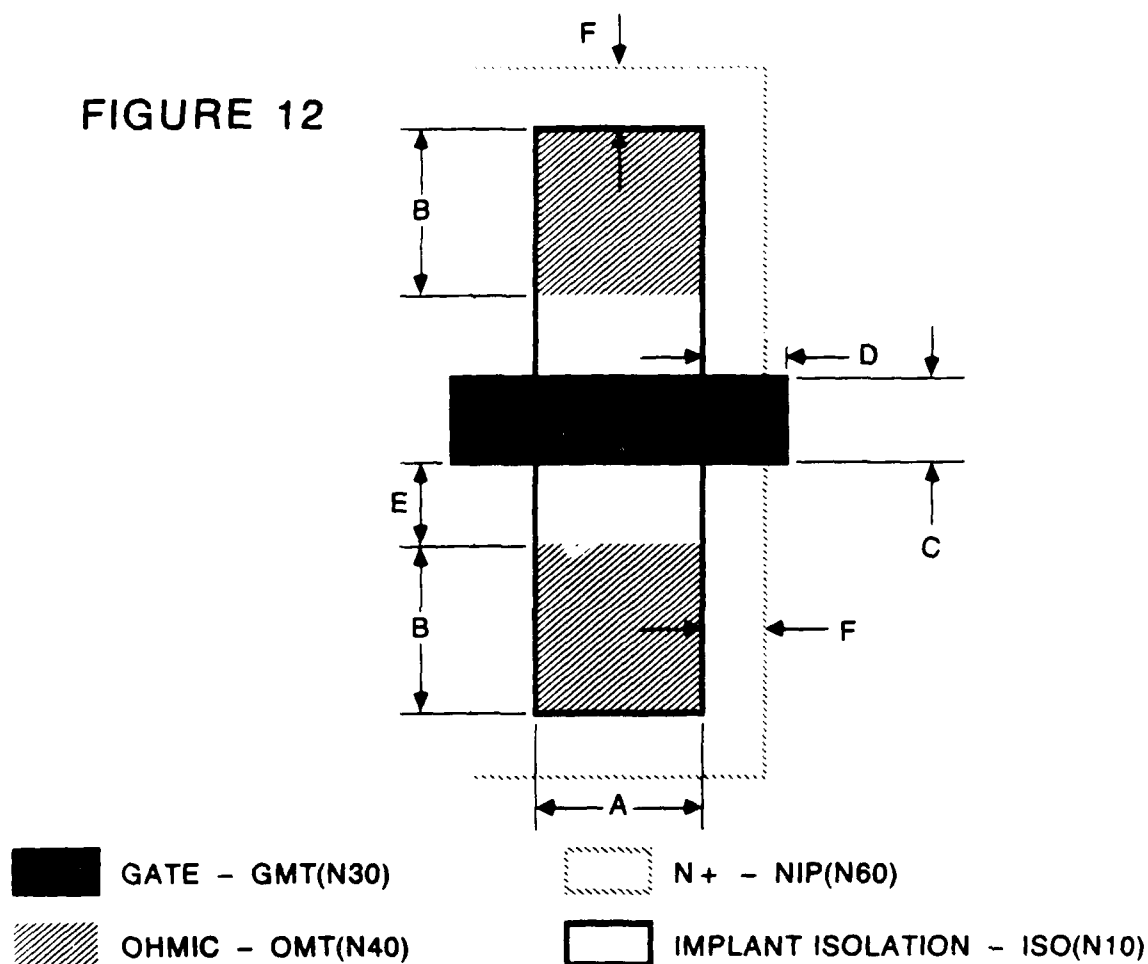


FIGURE 11

IMPLANT ISOLATED SARGIG/HFET 2.0 μ m DESIGN RULES
SARGIC HFET IMPLANT ISOLATED DEVICE GEOMETRY DESIGN RULES

FIGURE 12

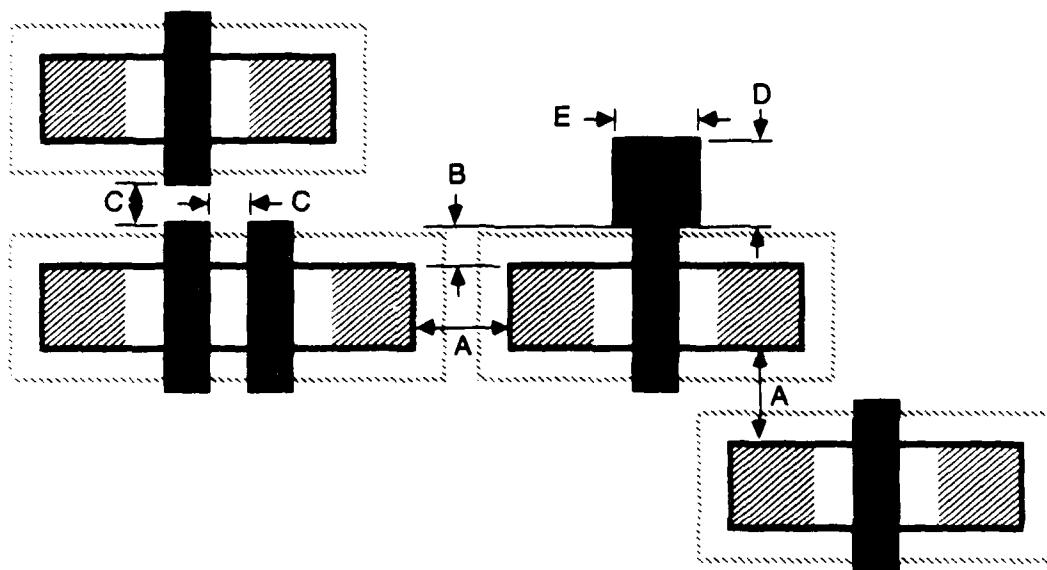


- A. MIN. DEVICE WIDTH - - 2.0 μ m
(DUE TO SCALING THE RECOMMENDED MIN. DEVICE WIDTH IS 3.0 μ m)
- B. MIN. SOURCE AND DRAIN LENGTH - - 2.0 μ m
- C. MIN. GATE LENGTH - - 1.0 μ m
- D. MIN. GATE EXTENSION BEYOND DEVICE - - 1.0 μ m
- E. MIN. OHMIC TO GATE METAL SPACING - - 1.0 μ m
- F. MIN. N+ EXTENSION BEYOND DEVICE - - 0.75 μ m
- G. ALL GATES MUST BE ORIENTED IN A SINGLE DIRECTION

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IMPLANT ISOLATED SARGIG/HFET 2.0 μ m DESIGN RULES DEVICE AND GATE SPACING DESIGN RULES

FIGURE 13



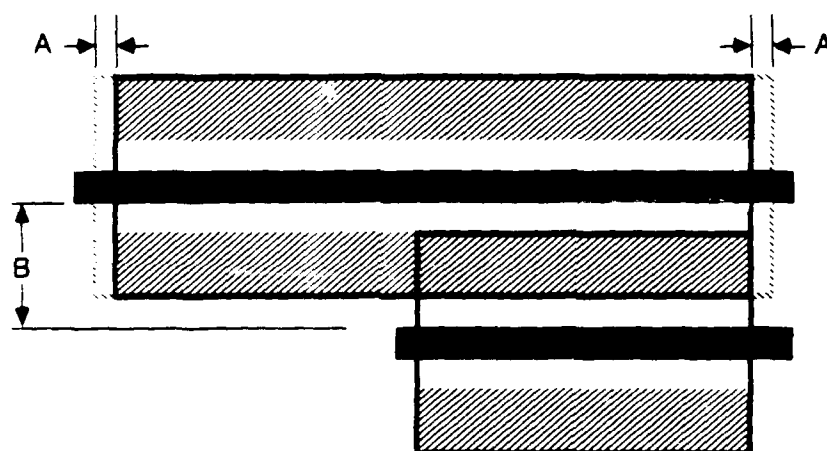
- GATE - GMT(N30)
- OHMIC - OMT(N40)
- N+ - NIP(N60)
- ISOLATION - ISO(N10)





- A. MIN. DEVICE TO DEVICE SPACING - - 2.0 μ m
- B. MIN. DEVICE TO GATE TAB SPACING - - 1.0 μ m
- C. MIN. GATE TO GATE SPACING - - 2.0 μ m
- D. MIN. GATE TAB WIDTH - - 2.0 μ m
- E. MIN. GATE TAB LENGTH - - 2.0 μ m

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IMPLANT ISOLATED SARGIG/HFET 2.0 μ m DESIGN RULES EHFET TUB DESIGN RULES

FIGURE 14



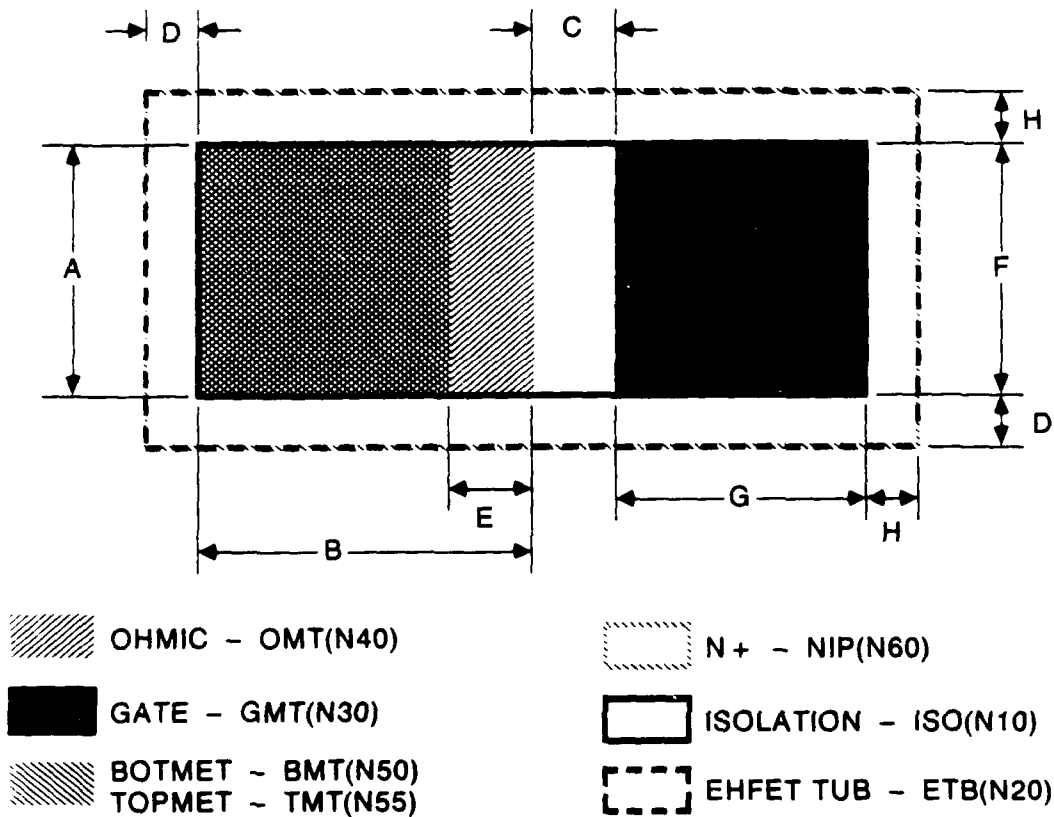
-  ISOLATION - ISO(N10)
-  EHFET TUB - ETB(N20)
-  GATE - GMT(N30)
-  OHMIC - OMT(N40)

- A. MIN. EHFET TUB EXTENSION BEYOND DEVICE WIDTH - - 0.75 μ m
- B. MIN. SPACING BETWEEN EHFET AND DHFET GATES - - 4.0 μ m

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IMPLANT ISOLATED SARGIG/HFET 2.0 μ m DESIGN RULES EHFET TUB DIODE DESIGN RULES

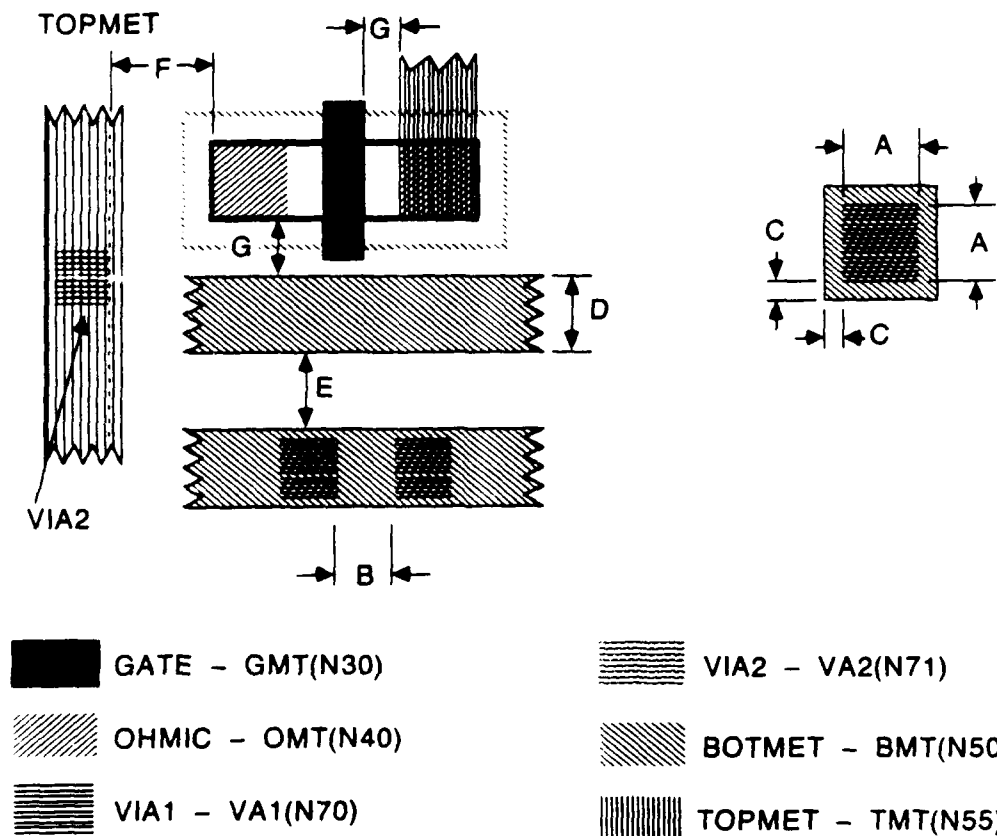
FIGURE 15



- A. MIN. DIODE WIDTH - - 2.0 μ m
(DUE TO SCALING THE RECOMMENDED MIN. DIODE WIDTH IS 3.0 μ m)
- B. MIN. OHMIC CONTACT LENGTH - - 3.0 μ m
- C. MIN. GATE TO OHMIC SPACING - - 1.0 μ m
- D. MIN. N+ EXTENSION BEYOND DEVICE - - 0.75 μ m
- E. MIN. BOTMET PULL-BACK FROM OHMIC - - 1.0 μ m
- F. MIN. GATE CONTACT WIDTH - - 2.0 μ m
- G. MIN. GATE CONTACT LENGTH - - 2.0 μ m
- H. MIN. E-FET TUB EXTENSION BEYOND DIODE EDGE - - 0.75 μ m

IMPLANT ISOLATED SARGIC/HFET 2.0 μ m DESIGN RULES VIA AND INTERCONNECT DESIGN RULES

FIGURE 16

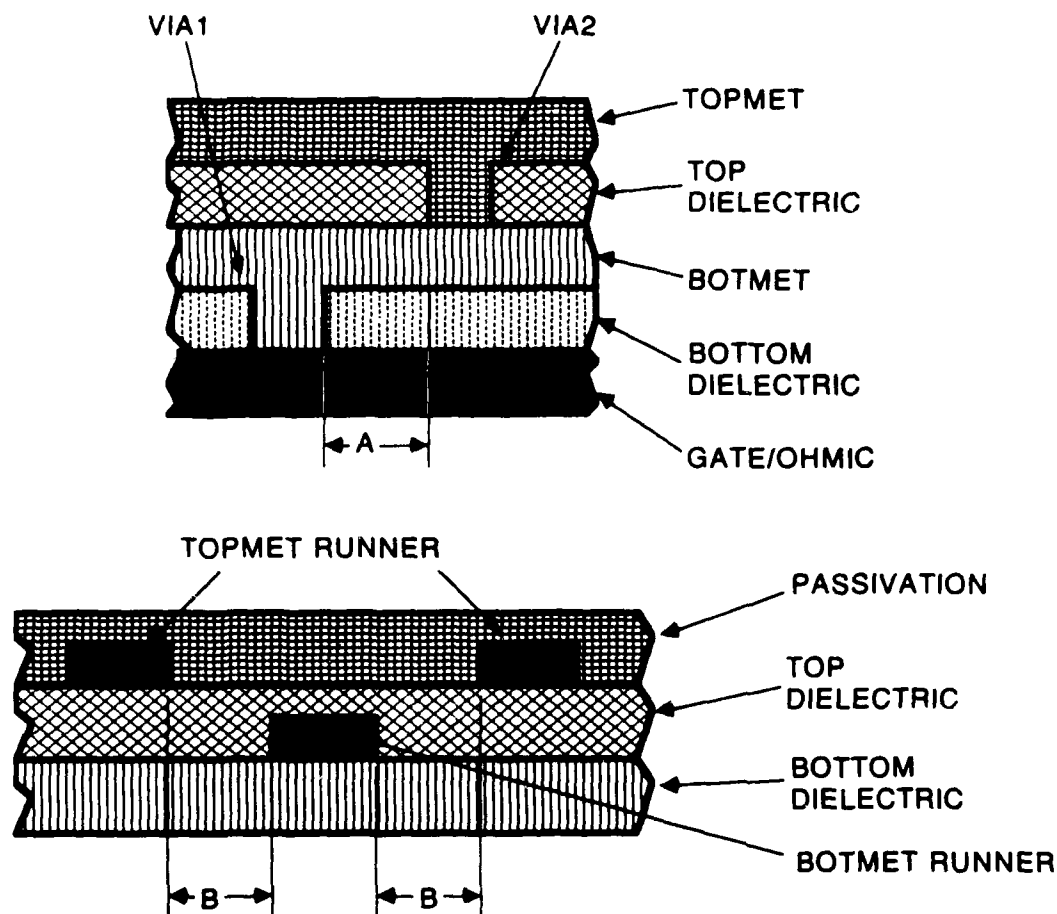


- A. MIN. CONTACT AREA (A X A) - - 1.5 X 1.5 μ m
- B. MIN. CONTACT SPACING - - 1.5 μ m
- C. MIN. METAL OVERLAP BEYOND CONTACT - - 0.25 μ m
- D. MIN. METAL WIDTH - - 2.0 μ m
- E. MIN. METAL SPACING - - 2.0 μ m
- F. MIN. VIA2 TO DEVICE SPACING - - 1.5 μ m
- G. MIN. SPACING BETWEEN BOTMET OR TOPMET TO DEVICE CHANNEL - - 1.0 μ m
- H. WHEN USING GATE/OHMIC FOR INTERCONNECT FOLLOW BOTMET/TOPMET INTERCONNECT DESIGN RULES (i.e. 2.0 μ m MIN. LINES & SPACES),
- I. NO TOPMET OR BOTMET ALLOWED OVER THE DEVICE GATE
- J. ALL INTERCONNECT MUST BE ORIENTED 0, OR 90° WITH RESPECT TO THE GATE

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IMPLANT ISOLATED SARGIC/HFET 2.0 μ m DESIGN RULES
TOPMET/BOTMET VIA AND INTERCONNECT DESIGN RULES

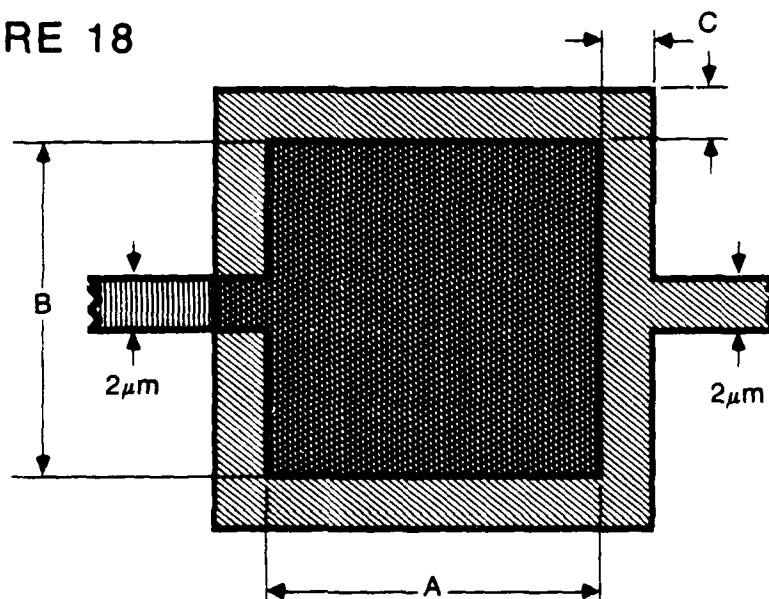
FIGURE 17



- A. MIN. SPACING BETWEEN TOPMET/BOTMET VIAS -- 1.5 μ m
B. MIN. SPACING BETWEEN PARALLEL TOPMET AND BOTMET
RUNNERS -- 1.0 μ m

IMPLANT ISOLATED SARGIG/HFET 2.0 μ m DESIGN RULES
CAPACITOR DESIGN RULES

FIGURE 18

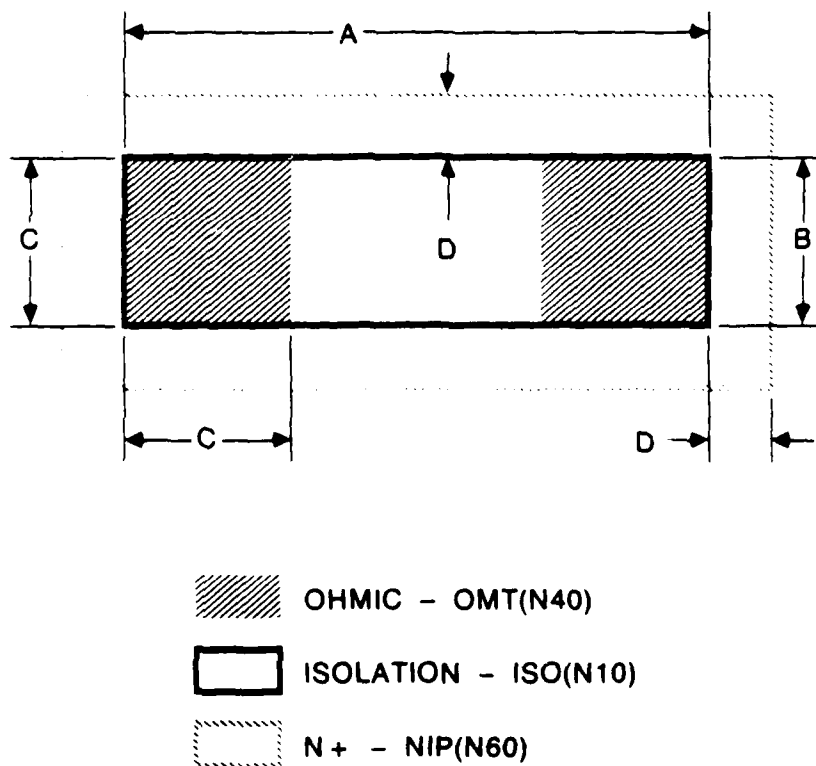


 BOTMET - N50
 TOPMET - N55

- A. MIN. CAPACITOR LENGTH - - 2.0 μ m
- B. MIN. CAPACITOR WIDTH - - 2.0 μ m
- C. MIN. BOTMET EXTENSION BEYOND TOPMET - - 1.0 μ m

IMPLANT ISOLATED SARGIG/HFET 2.0 μ m DESIGN RULES
N+ IMPLANTED RESISTOR DESIGN RULES

FIGURE 19

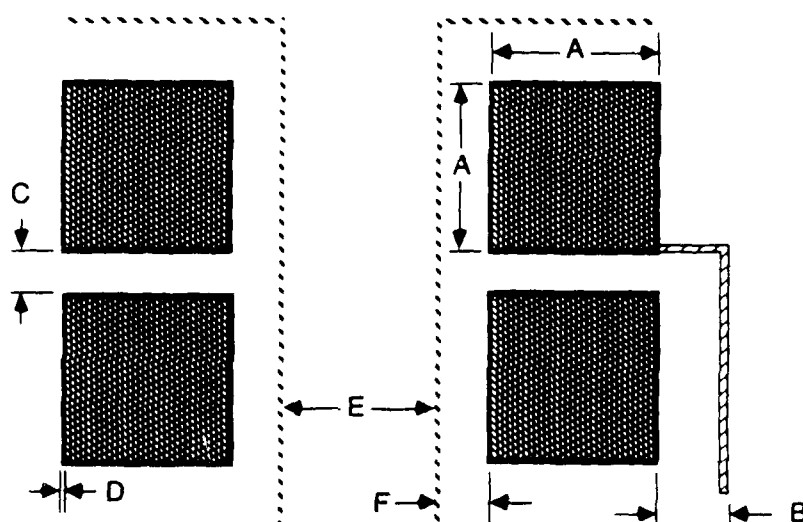
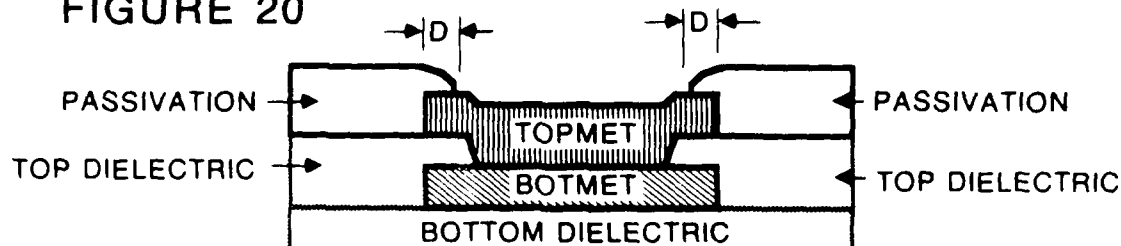


- A. MIN. RESISTOR LENGTH - - 6.0 μ m
- B. MIN. RESISTOR WIDTH - - 2.0 μ m
- C. MIN. CONTACT AREA (C X C) - - 2.0 X 2.0 μ m
- D. MIN. N+ EXTENSION BEYOND RESISTOR - - 0.75 μ m

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IMPLANT ISOLATED SARGIG/HFET 2.0 μ m DESIGN RULESBONDING PAD DESIGN RULES

FIGURE 20



TOPMET - TMT(N55)

PASSIVATION - PAS(N79)

BOTMET - BMT(N50)

VIA2 - VA2(N71)

- A. MIN. PAD SIZE - - 100 μ m
- B. MIN. PAD TO METAL SPACING - - 25 μ m
- C. MIN. PAD TO PAD SPACING - - 25 μ m
- D. MIN. METAL OVERLAP BEYOND VIA2/PASSIVATION - - 2.5 μ m
- E. MIN. DICING LANE WIDTH - - 120 μ m
- F. MIN. SPACING FROM PAD TO EDGE OF DICING LANE - - 25 μ m

TABLE 1

PROCESS SPECIFICATIONS:

The following table describes the minimum, nominal, and maximum parameter values for the DIGITAL SARGIC process.

<u>SYMBOL</u>	<u>PARAMETER NAME</u>	<u>MIN.</u>	<u>NOM.</u>	<u>MAX.</u>	<u>UNITS</u>
RSNIP*	sheet R of N+	360	560	770	ohms/sq
RSGMT	sheet R of GMT	4.0	4.5	5.0	ohms/sq
RSOMT	sheet R of OMT	0.32	0.47	0.62	ohms/sq
RSBMT	sheet R of BMT	0.036	0.048	0.060	ohms/sq
RSTMT	sheet R of TMT	0.027	0.036	0.045	ohms/sq
RC EHFET	EHFET ohmic contact resistance per unit width	50	190	430	ohms/ μ m
RC DHFET	DHFET ohmic contact resistance per unit width	140	470	800	ohms/ μ m
I _{ISO}	Isolation Current at 20 μ m spacing and +2.0V per unit width		31	91	pA/ μ m

* NOTE: THIS IS THE SHEET RESISTANCE OF THE DHFET N+ IMPLANT

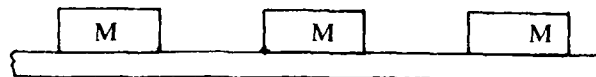
The following table gives the nominal values of gate, ohmic, and interconnect metal capacitances.

TABLE 2

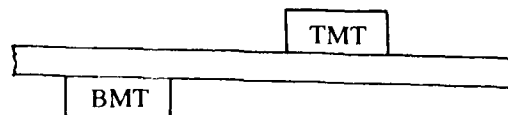
<u>SYMBOL</u>	<u>PARAMETER NAME</u>	<u>MIN.</u>	<u>NOM.</u>	<u>MAX</u>	<u>UNITS</u>
CMIM	MIM cap/unit area (TMT to BMT)		0.111		fF/ μm^2
CTO	cap/unit area of TMT to OMT		0.055		fF/ μm^2
CTG	cap/unit area of TMT to GMT		0.072		fF/ μm^2
CBO	cap/unit area of BMT to OMT		0.11		fF/ μm^2
CBG	cap/unit area of BMT to GMT		0.146		fF/ μm^2
CCG ¹	cap/unit length of GMT to GMT		0.142		fF/ μm
COO ¹	cap/unit length of OMT to OMT		0.107		fF/ μm
CBB ¹	cap/unit length of BMT to BMT		0.162		fF/ μm
CTT ¹	cap/unit length of TMT to TMT		0.147		fF/ μm
CTB ²	cap/unit length of TMT to BMT		1.82		fF/ μm
CTB ³	cap/unit length of TMT to BMT		1.41		fF/ μm
CBT ³	cap/unit length of BMT to TMT		1.71		fF/ μm

NOTES: Notes 1 to 3 above refer to the following arrangements of interconnect and gate/ohmic metals.

CASE 1:



CASE 2:



CASE 3:

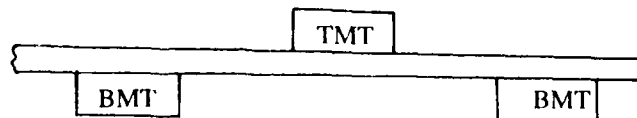


TABLE 3
HFET DEVICE BREAKDOWN VOLTAGE

	<u>MIN</u>	<u>TYP</u>	<u>MAX</u>
EHFET TUB DIODE:			
V_F at $I_F=10\mu A/\mu m$		0.78V	
V_R	10V		
I_S at $V_R=3V$		2.0 μA	
EHFET:			
BV_{DGO} (Open Source)	9.0V		
BV_{SGO} (Open Drain)	10V		
V_F (Drain & Source Connected) at $I_G=10\mu A/\mu m$		0.8V	
DHFET:			
BV_{DGO} (Open Source)	10V		
BV_{SGO} (Open Drain)	10V		
V_F (Drain & Source Connected) at $I_G=10\mu A/\mu m$	2.0V		

TABLE 4
MASK LEVELS

PROCESSED LEVELS:

<u>LEVEL NAME</u>	<u>DESCRIPTION</u>
ETB	EHFET TUB
ETBLITHO	EHFET TUB Lithography Evaluation Features
ETBNOGS	EHFET TUB Uncompensated Features
ISO	ISOLATION
ISODI	ISOLATION for diodes
ISORES	ISOLATION for resistors
ISOLITHO	ISOLATION Lithography Evaluation Features
ISONOGS	ISOLATION Uncompensated Features
GMT	GATE METAL for Interconnect Runners
GMTE	GATE METAL for Enhancement FETs
GMTD	GATE METAL for Depletion FETs
GMTLITHO	GATE METAL Lithography Evaluation Features
GMTNOGS	GATE METAL Uncompensated Features
NIP	N+ Implant
NIPLITHO	N+ Implant Lithography Evaluation Features
NIPNOGS	N+ Implant Uncompensated Features
OMT	OHMIC METAL
OMTLITHO	OHMIC METAL Lithography Evaluation Features
OMTNOGS	OHMIC METAL Uncompensated Features
VA1	VIA1
VA1LITHO	VIA1 Lithography Evaluation Features
VA1NOGS	VIA1 Uncompensated Features
BMT	BOTTOM METAL
BMTCP	BOTTOM METAL for capacitors
BMTBP	BOTTOM METAL for bond pads
BMTLITHO	BOTTOM METAL Lithography Evaluation Features
BMTNOGS	BOTTOM METAL Uncompensated Features
VA2	VIA2
VA2BP	VIA2 for bond pads
VA2LITHO	VIA2 Lithography Evaluation Features
VA2NOGS	VIA2 Uncompensated Features

TABLE 4
MASK LEVELS

PROCESSED LEVELS:

<u>LEVEL NAME</u>	<u>DESCRIPTION</u>
TMT	TOP METAL
TMTCP	TOP METAL for capacitors
TMTBP	TOP METAL for bond pads
TMTLITHO	TOP METAL Lithography Evaluation Features
TMTNOGS	TOP METAL Uncompensated Features
PAS	PASSIVATION
PASNOGS	PASSIVATION Uncompensated Features

NON-PROCESSED LEVELS:

<u>LEVEL NAME</u>	<u>DESCRIPTION</u>
CELLOUT	CELL OUTLINE
LABOMT	OHMIC METAL LABEL
LABGMT	GATE METAL LABEL
LABBMTP	BOTTOM METAL POWER BUS LABEL
LABBMT	BOTTOM METAL LABEL
LABTMTP	TOP METAL POWER BUS LABEL
LABTMT	TOP METAL LABEL
OUT	MISCELLANEOUS OUTLINES
TEXT	MISCELLANEOUS TEXT
LABGM1	GATE MATRIX LABEL 1
LABGM2	GATE MATRIX LABEL 2
LABGM3	GATE MATRIX LABEL 3

TABLE 5
VERSION 1 ISSUE 2.6

GaAs SARGIC/SDHT TWO LEVEL METAL 2.0 MICRON DESIGN RULES

IMPLANT ISOLATED DEVICE GEOMETRY DESIGN RULES

1. Minimum Device Width (A)	2.0 μ m	Fig. 12/A
2. Minimum Source and Drain	2.0 μ m	Fig. 12/B
3. Minimum Gate Length	1.0 μ m	Fig. 12/C
4. Minimum Gate Extension Beyond Device	1.0 μ m	Fig. 12/D
5. Minimum Ohmic to Gate Metal Spacing	1.0 μ m	Fig. 12/E
6. Minimum N+ Extension Beyond Device	0.75 μ m	Fig. 12/F
7. All Gates Must be Oriented In A Single Direction		

DEVICE AND GATE SPACING DESIGN RULES

8. Minimum Device to Device Spacing	2.0 μ m	Fig. 13/A
9. Minimum Device to Gate Tab Spacing	1.0 μ m	Fig. 13/B
10. Minimum Gate to Gate Spacing	2.0 μ m	Fig. 13/C
11. Minimum Gate Tab Width	2.0 μ m	Fig. 13/D
12. Minimum Gate Tab Length	2.0 μ m	Fig. 13/E

EFET TUB DESIGN RULES

13. Minimum EFET Tub Extension	0.75 μ m	Fig. 14/A
14. Minimum Spacing Between E-FET and D-FET Gates with Shared Source	4.0 μ m	Fig. 14/B

DIODE DESIGN RULES

15. Minimum Diode Width (A)	2.0 μ m	Fig. 15/A
16. Minimum Diode Contact Length	3.0 μ m	Fig. 15/B
17. Minimum Gate to Ohmic Spacing	1.0 μ m	Fig. 15/C
18. Minimum N+ Extension Beyond Device	0.75 μ m	Fig. 15/D
19. Minimum Botmet Pull-back From Ohmic	1.0 μ m	Fig. 15/E
20. Minimum Gate Contact Width	2.0 μ m	Fig. 15/F
21. Minimum Gate Contact Length	2.0 μ m	Fig. 15/G
22. Minimum EFET Tub Extension Beyond Diode Edge	0.75 μ m	Fig. 15/H

(A) Due to scaling, the recommended minimum device width is 3.0 μ m.

VIA AND INTERCONNECT DESIGN RULES

TABLE 5
VERSION 1 ISSUE 2.6

23. Via Contact Area	1.5 x 1.5 μ m	Fig. 16/A
24. Minimum Contact Spacing	1.5 μ m	Fig. 16/B
25. Minimum Metal Overlap Beyond Contact	0.25 μ m	Fig. 16/C
26. Minimum Metal Width	2.0 μ m	Fig. 16/D
27. Minimum Metal Spacing	2.0 μ m	Fig. 16/E
28. Minimum Spacing Topmet/Botmet Vias	1.5 μ m	Fig. 16/F
29. Minimum VIA2 to Device Spacing	1.0 μ m	Fig. 16/H
30. When using Gate/Ohmic for Interconnect follow Botmet/Topmet Interconnect Design Rules. (i.e. 2.0 μ m Min. Lines and Spaces)		
31. No Botmet or Topmet Allowed Over Device Gate.		
32. All Interconnect Must Be Oriented 0, 45, or 90 Degrees with Respect to Gate.		

TOPMET/BOTMET VIA AND INTERCONNECT DESIGN RULES

33. Minimum Spacing Between TOPMET/BOT VIAS	Fig. 17/A
34. Minimum Spacing Between Parallel TOPMET and BOTMET Runners	Fig. 17/B

CAPACITOR DESIGN RULES

35. Minimum Capacitor Length	2.0 μ m	Fig. 18/A
36. Minimum Capacitor Width		
37. Minimum Botmet/Extension beyond Topmet	1.0 μ m	Fig. 18/C

RESISTOR DESIGN RULES

38. Minimum Overall Resistor Length	74.0 μ m	Fig. 19/A
39. Minimum Resistor Width	2.0 μ m	Fig. 19/B
40. Minimum Contact Area	4.0 μ m sq.	Fig. 19/C
41. Minimum N+ Extension Beyond Resistor	0.75 μ m	Fig. 19/D
42. Minimum Final Resistor Length	70.0 μ m	Fig. 19/B

BONDING PAD DESIGN RULES

43. Minimum Pad Size	100 μ m sq.	Fig. 20/A
44. Minimum Pad to Metal Spacing	25 μ m	Fig. 20/B
45. Minimum Pad to Pad Spacing	25 μ m	Fig. 20/C
46. Minimum Metal Extension Beyond Via2/ Passivation	2.5 μ m	Fig. 20/D
47. Minimum Dicing Lane Width	120 μ m	Fig. 20/E
48. Minimum Pad to Dicing Lane Edge	25 μ m	Fig. 20/F

DEVICE TERMINAL CHARACTERISTICS

This section contains the nominal terminal characteristics of HFETs and schottky diodes at 25 and 125°C. The characteristics are modeled using AT&T's ADVICE circuit simulator and given in tabular and graphical format. They include current/voltage (I/V) and capacitance/voltage (C/V) data. The ADVICE models parameters were extracted from measured HFET and diode characteristics and fitted to the measurements.

Presently all integrated circuits including the DARPA standard cell library, are designed in the SARGIC/HFET process. Circuit functionality is verified using ADVICE. The DC and transient response of circuits is simulated using the ADVICE circuit simulator and correlated with the measured response.

All simulations at present use the nominal device models that have been extracted for EHFET, DHFET, and schottky diode devices. In future updates, the models will be expanded to include best, nominal, and worst case parameters. Also other model parameters will be added to cover temperatures below 25 and above 125°C.

SPICE circuit simulator model parameters for the SARGIC/HFET process are not planned for release at this time by AT&T. However, they can also be extracted from the tables and fitted to the data provided in this manual by interested SPICE users. Availability of ADVICE model parameters will give DoD contractors the ability to license ADVICE from AT&T.

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- Figure 34. I_g vs. V_{gs} for ed25 Diode Simulation at 25C (semilog).
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- Figure 37. I_g vs. V_{gs} for ed125 Diode Simulation at 125C (semilog).
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- Table 23. I_g vs. V_{gs} for ed125 Diode Simulation at 125C.
- Table 24. C vs. V_{gs} for ed125 Diode Simulation at 125C.

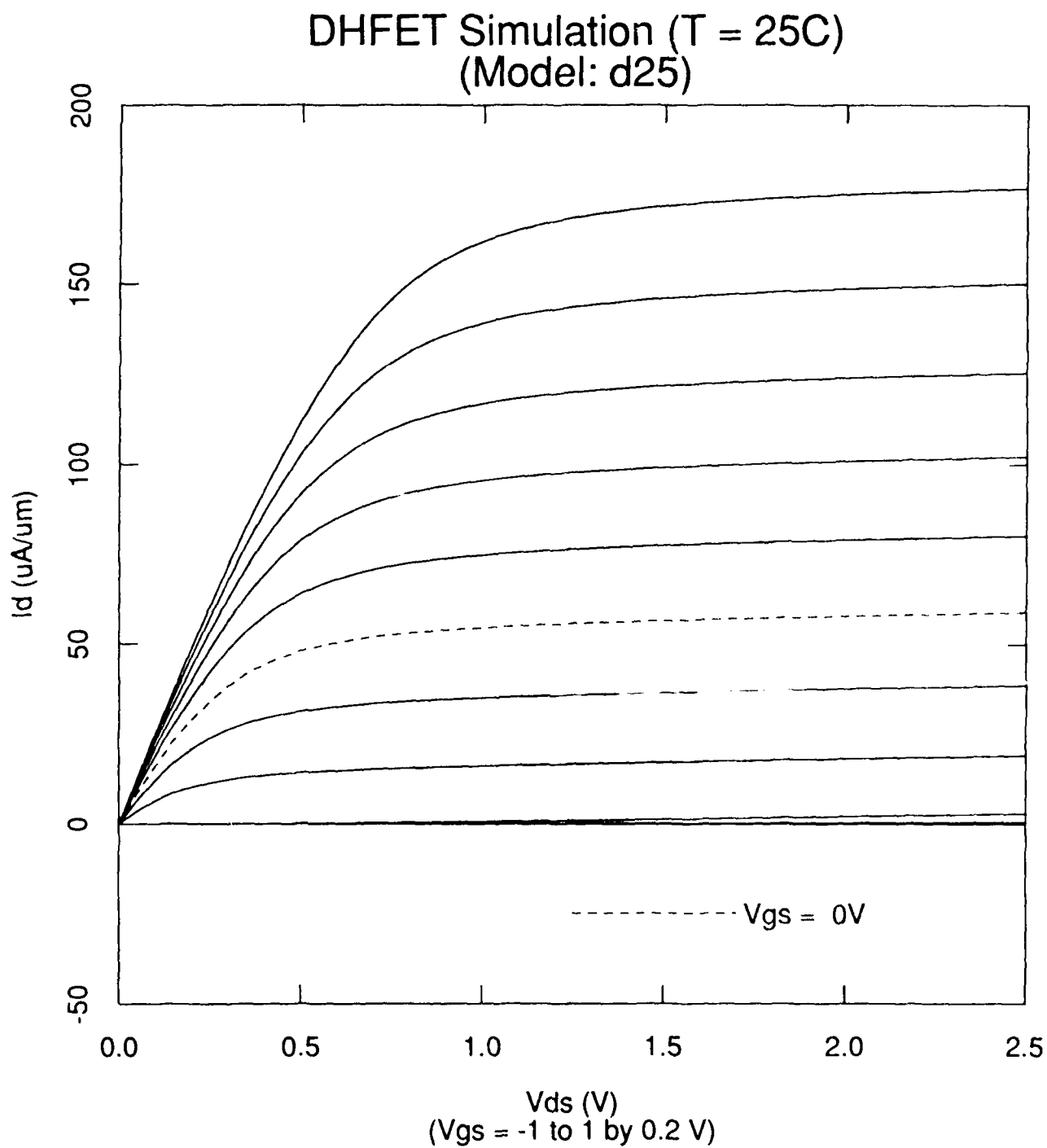


Figure 1. I_d vs. V_{ds} (V_{gs} stepped) for d25 DHFET Simulation at 25C.

DHFET Simulation (T = 25C)
(Model: d25)

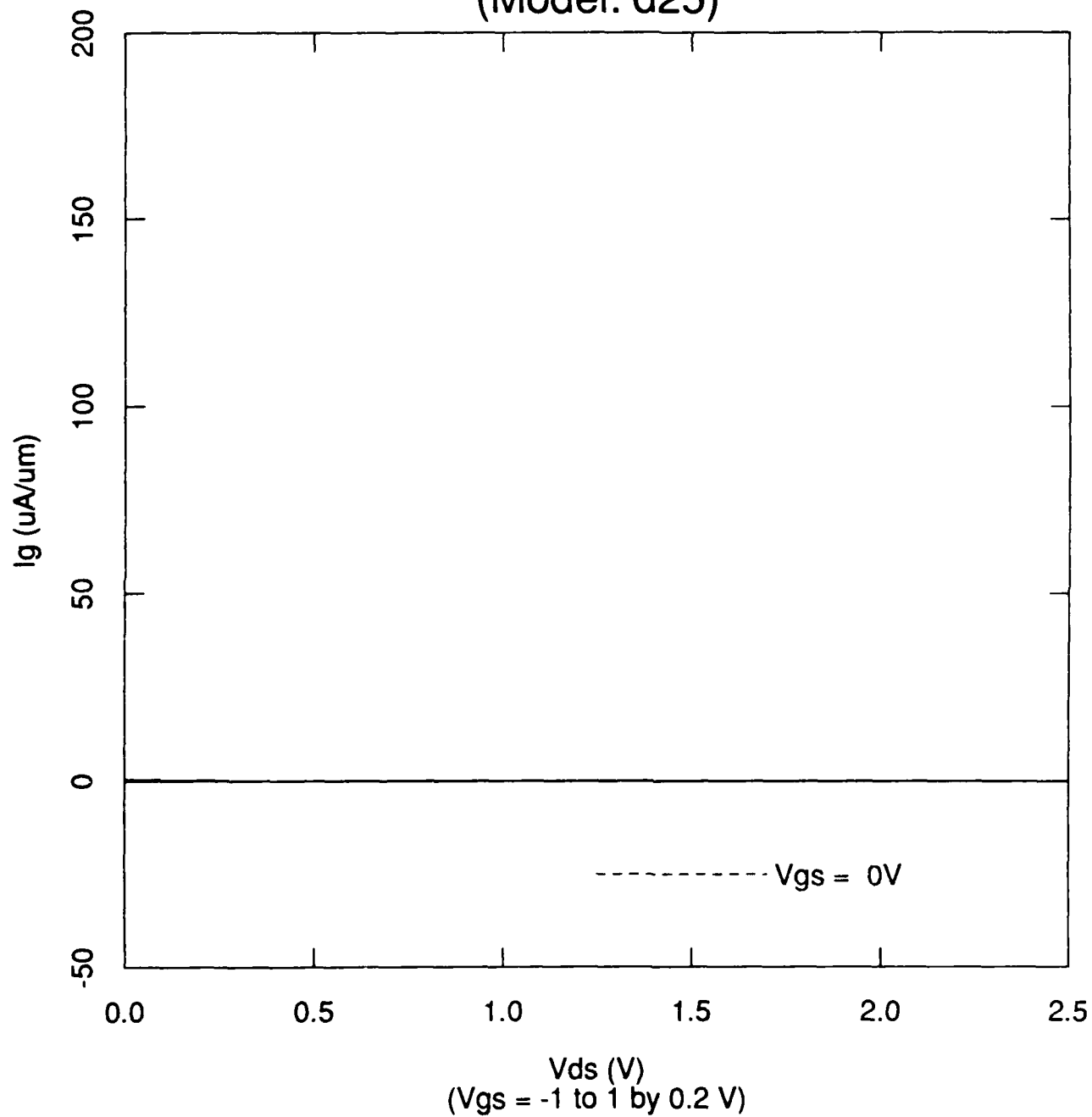


Figure 2. I_g vs. V_{ds} (V_{gs} stepped) for d25 DHFET Simulation at 25C.

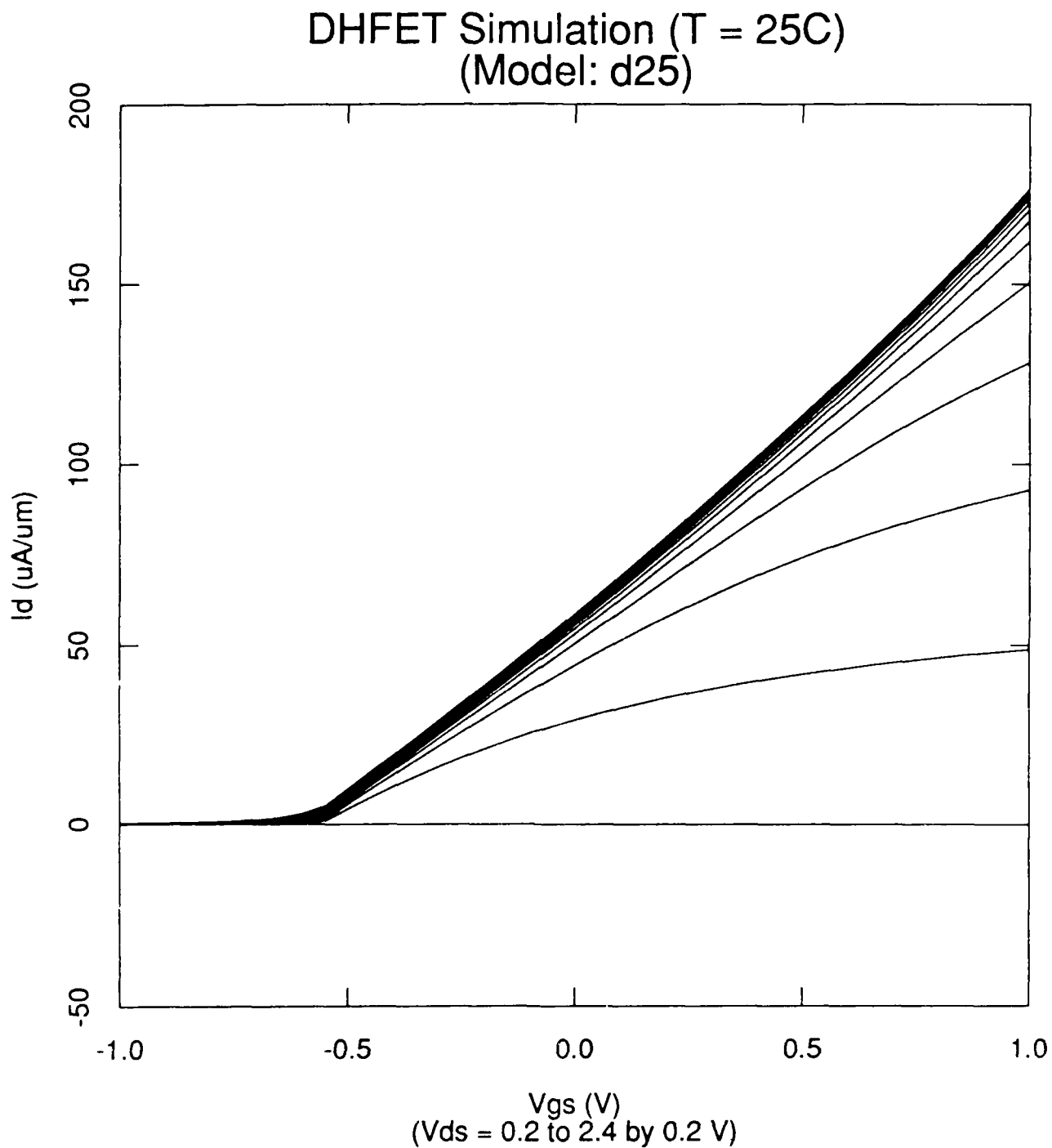


Figure 3. I_d vs. V_{gs} (V_{ds} stepped) for d25 DHFET Simulation at 25C.

DHFET Simulation (T = 25C)
(Model: d25)

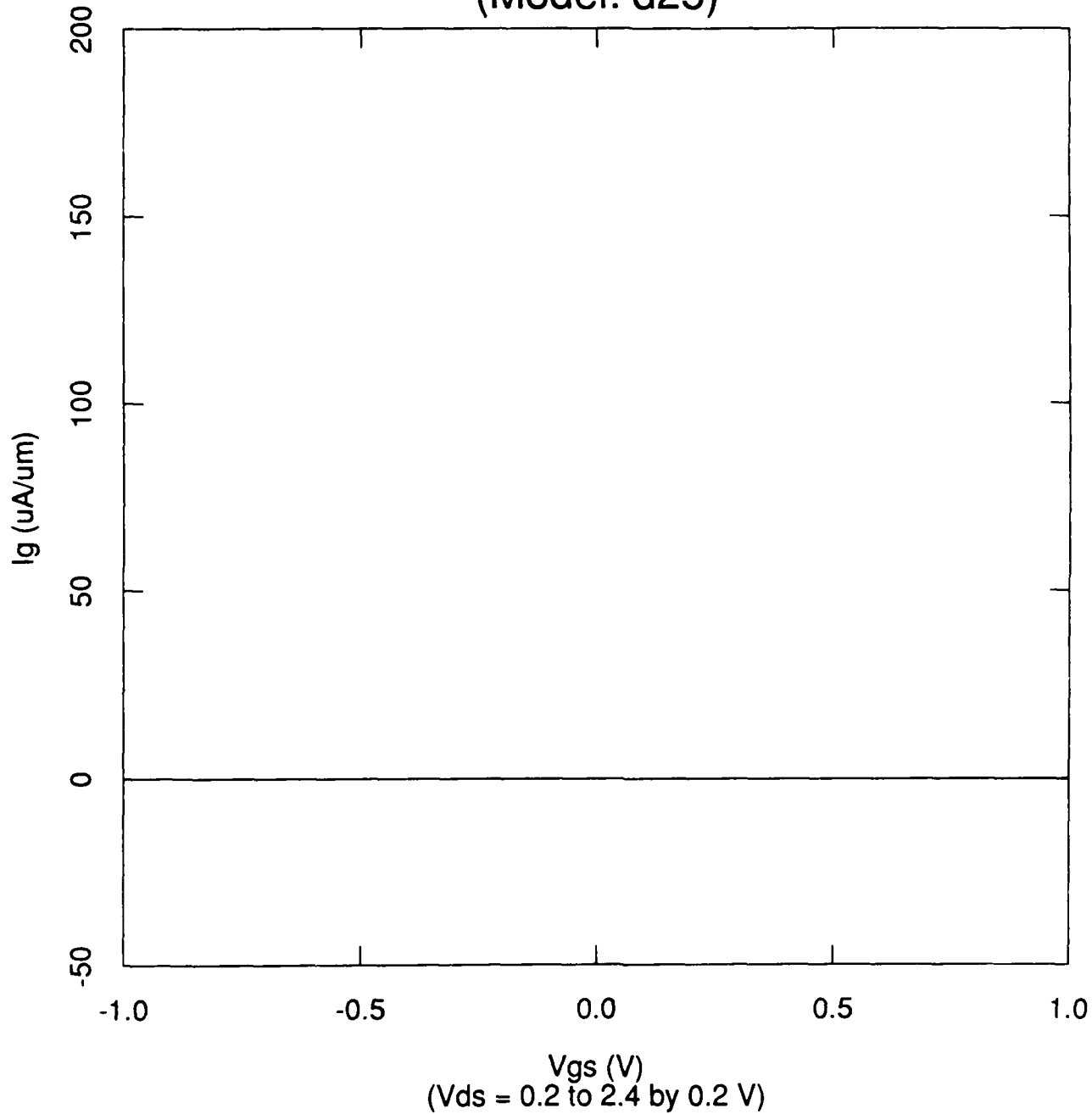


Figure 4. I_g vs. V_{gs} (V_{ds} stepped) for d25 DHFET Simulation at 25C.

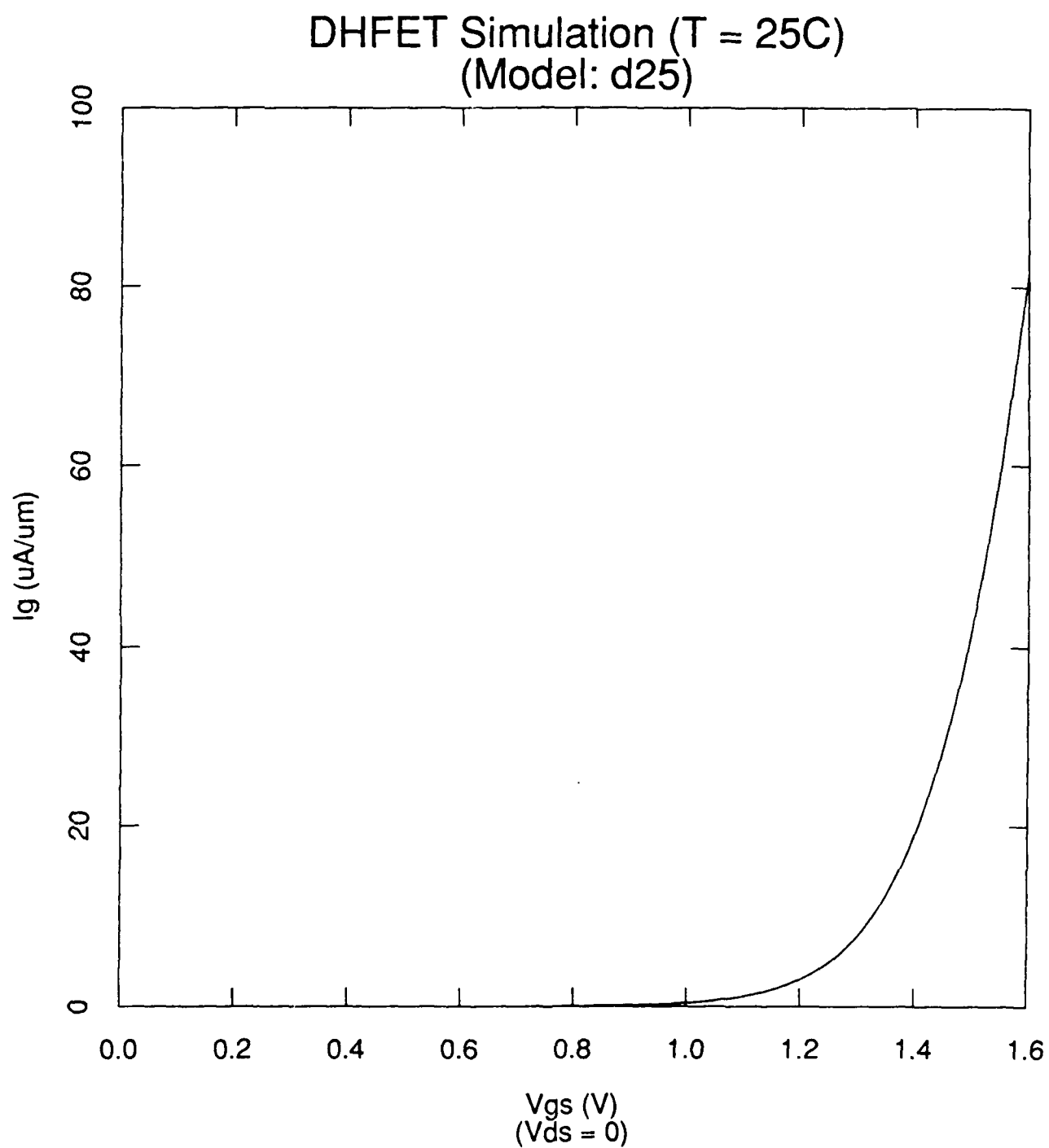


Figure 5. I_g vs. V_{gs} ($V_{ds} = 0$) for d25 DHFET Simulation at 25C.

DHFET Simulation (T = 25C)
(Model: d25)

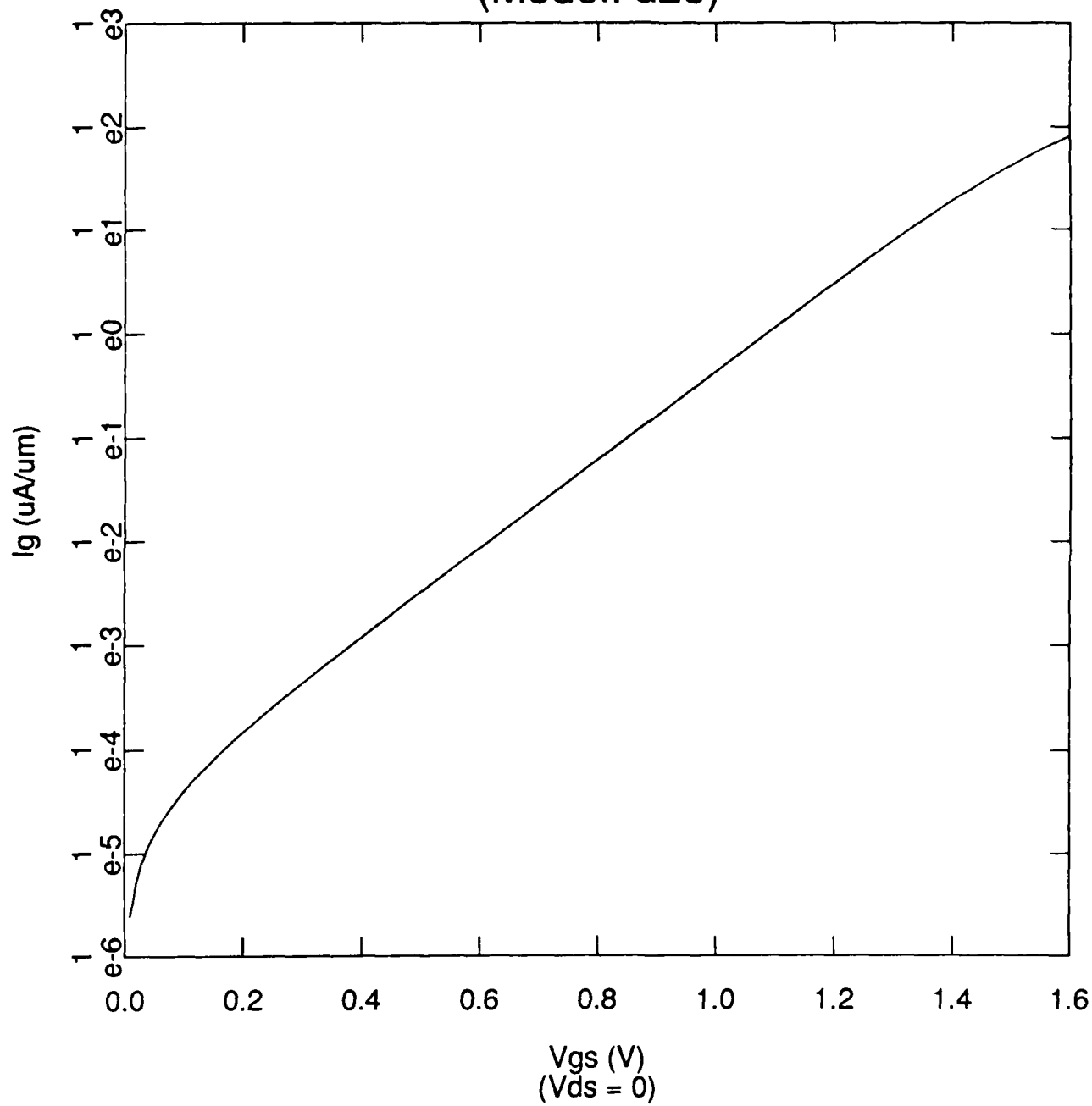


Figure 6. I_g vs. V_{gs} ($V_{ds} = 0$) for d25 DHFET Simulation at 25C (semilog).

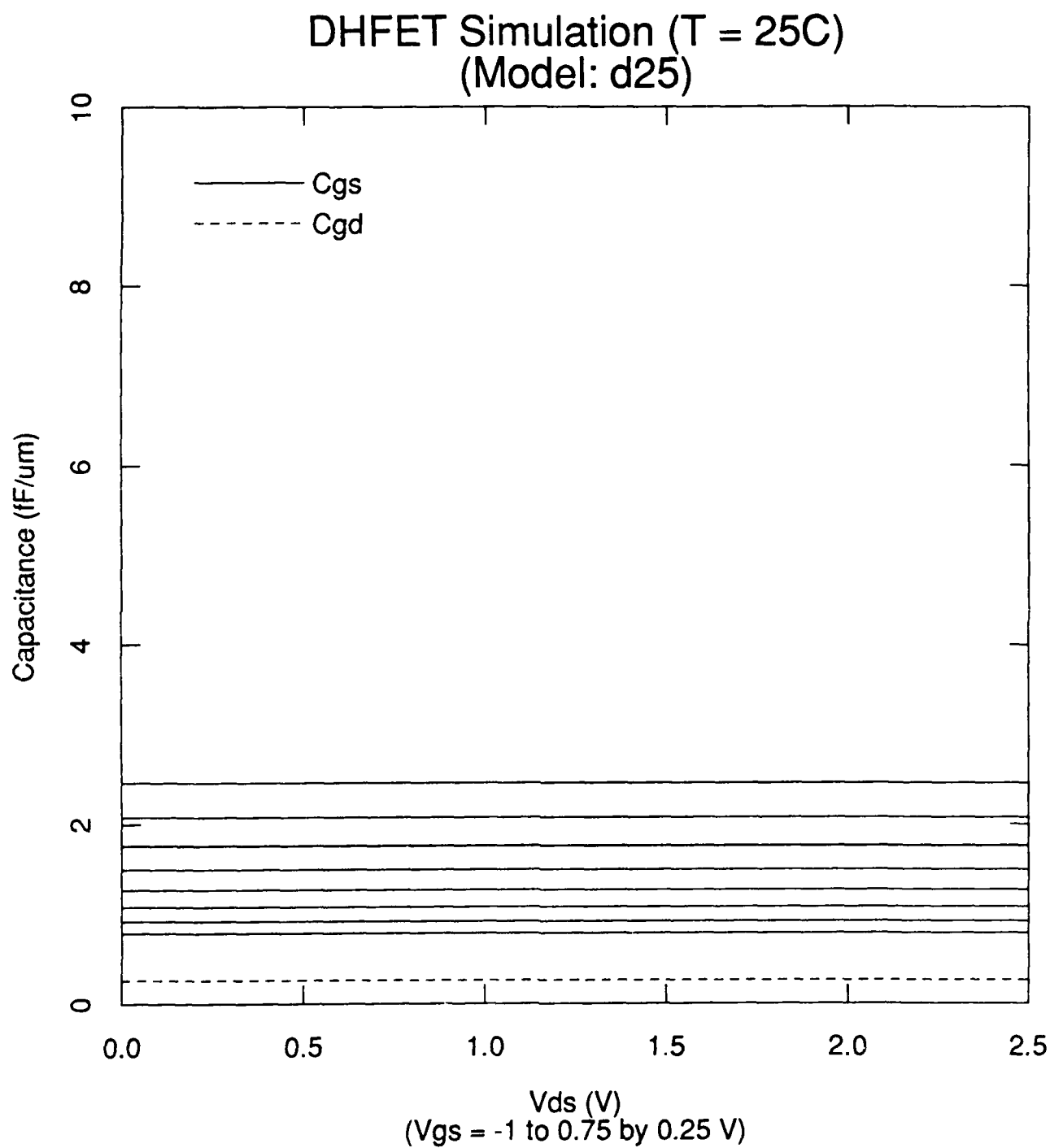


Figure 7. C_{gd} and C_{gs} vs. V_{ds} (V_{gs} stepped) for d25 DHFET Simulation at 25C.

DHFET Simulation ($T = 25\text{C}$)
(Model: d25)

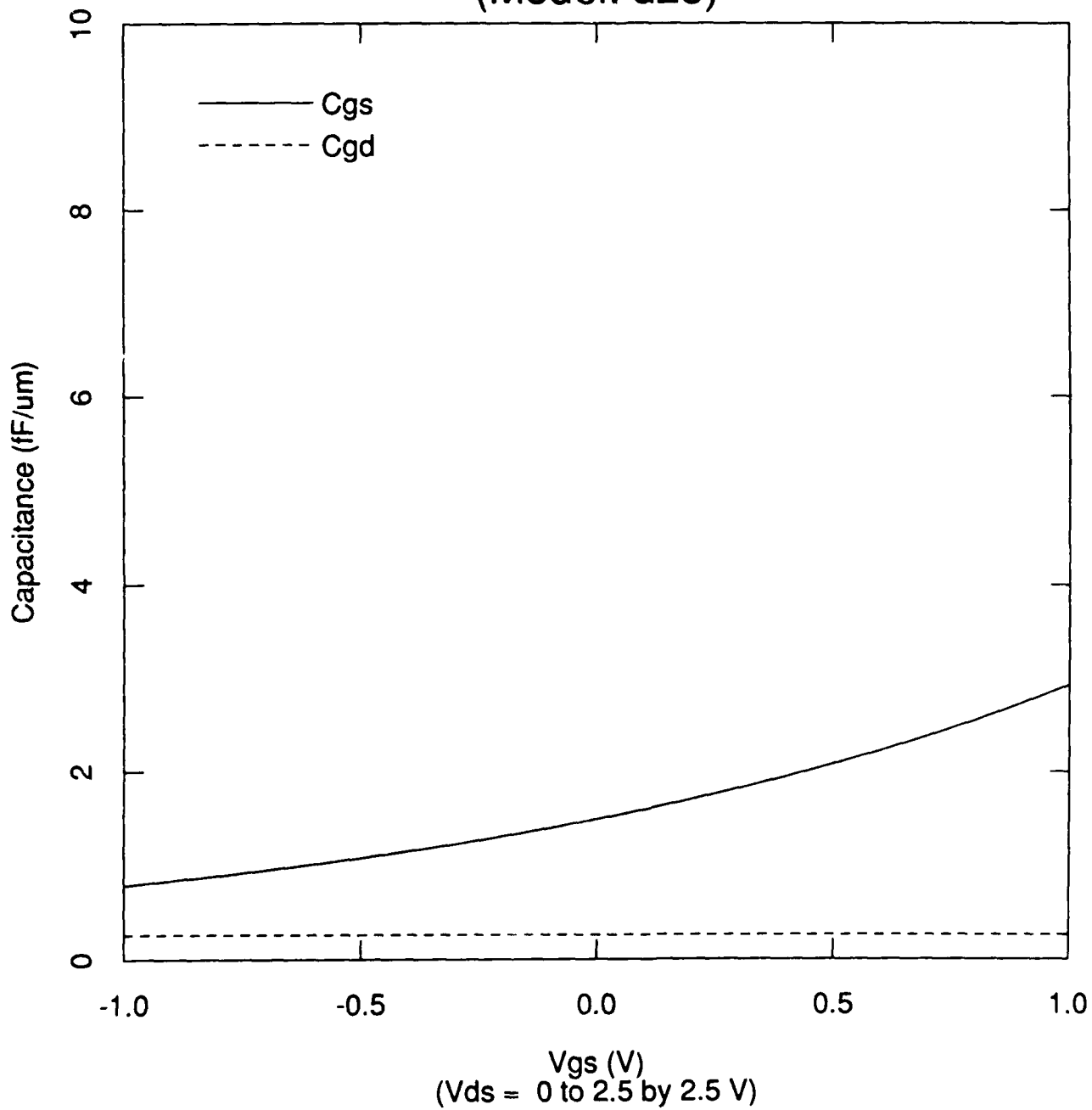


Figure 8. C_{gd} and C_{gs} vs. V_{gs} (V_{ds} stepped) for d25 DHFET Simulation at 25C.

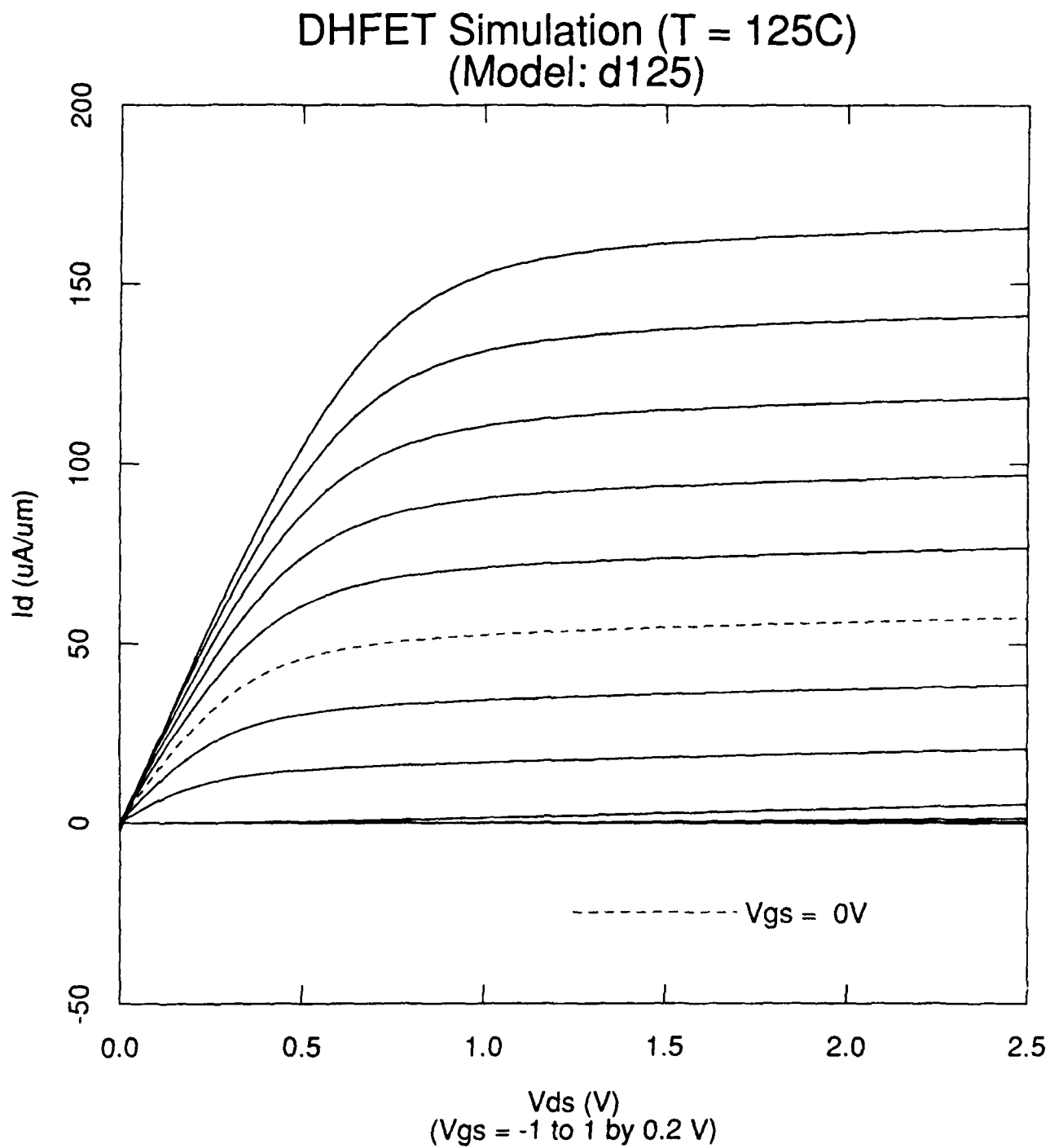


Figure 9. I_d vs. V_{ds} (V_{gs} stepped) for d125 DHFET Simulation at 125C.

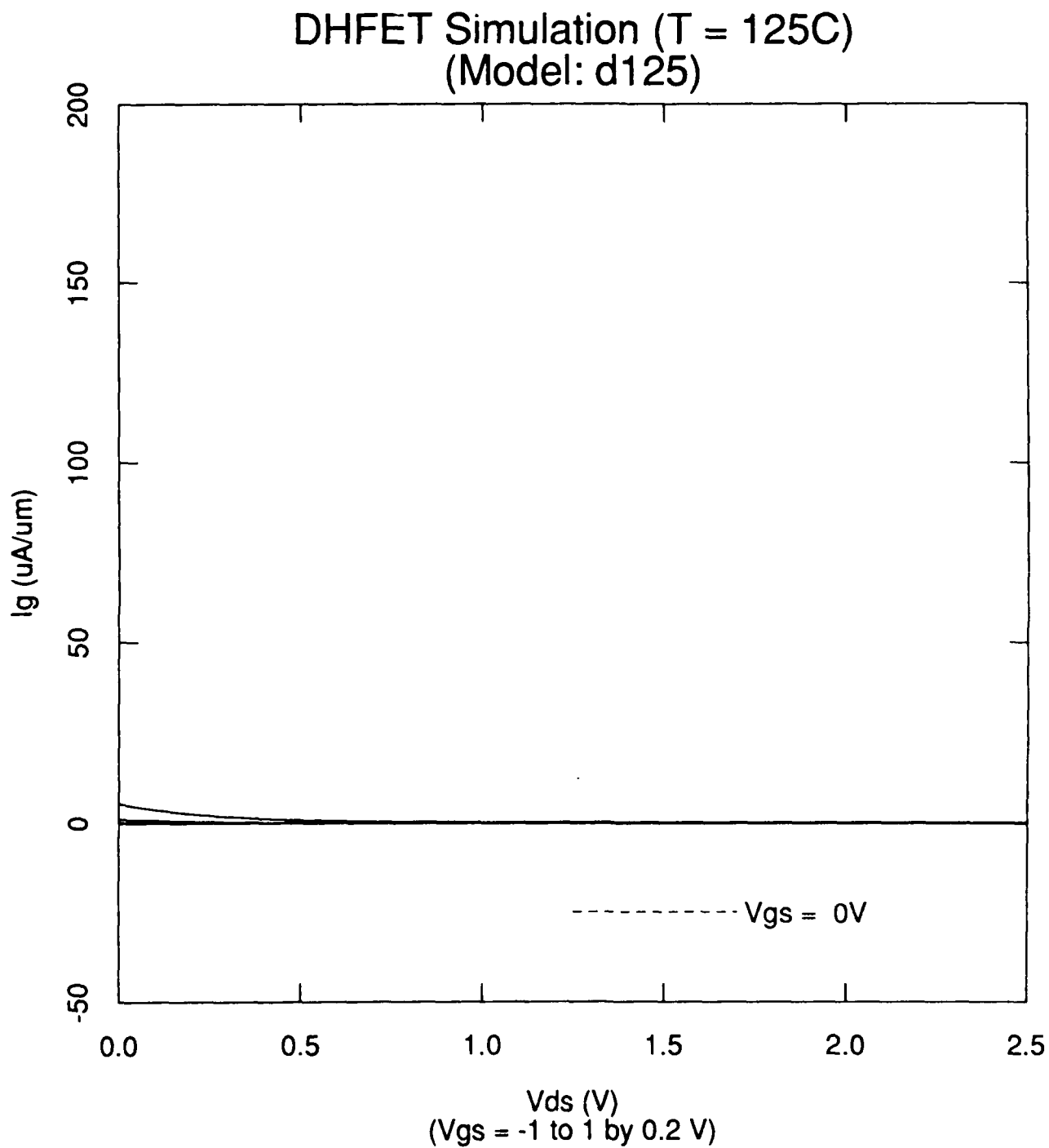


Figure 10. Ig vs. Vds (Vgs stepped) for d125 DHFET Simulation at 125C.

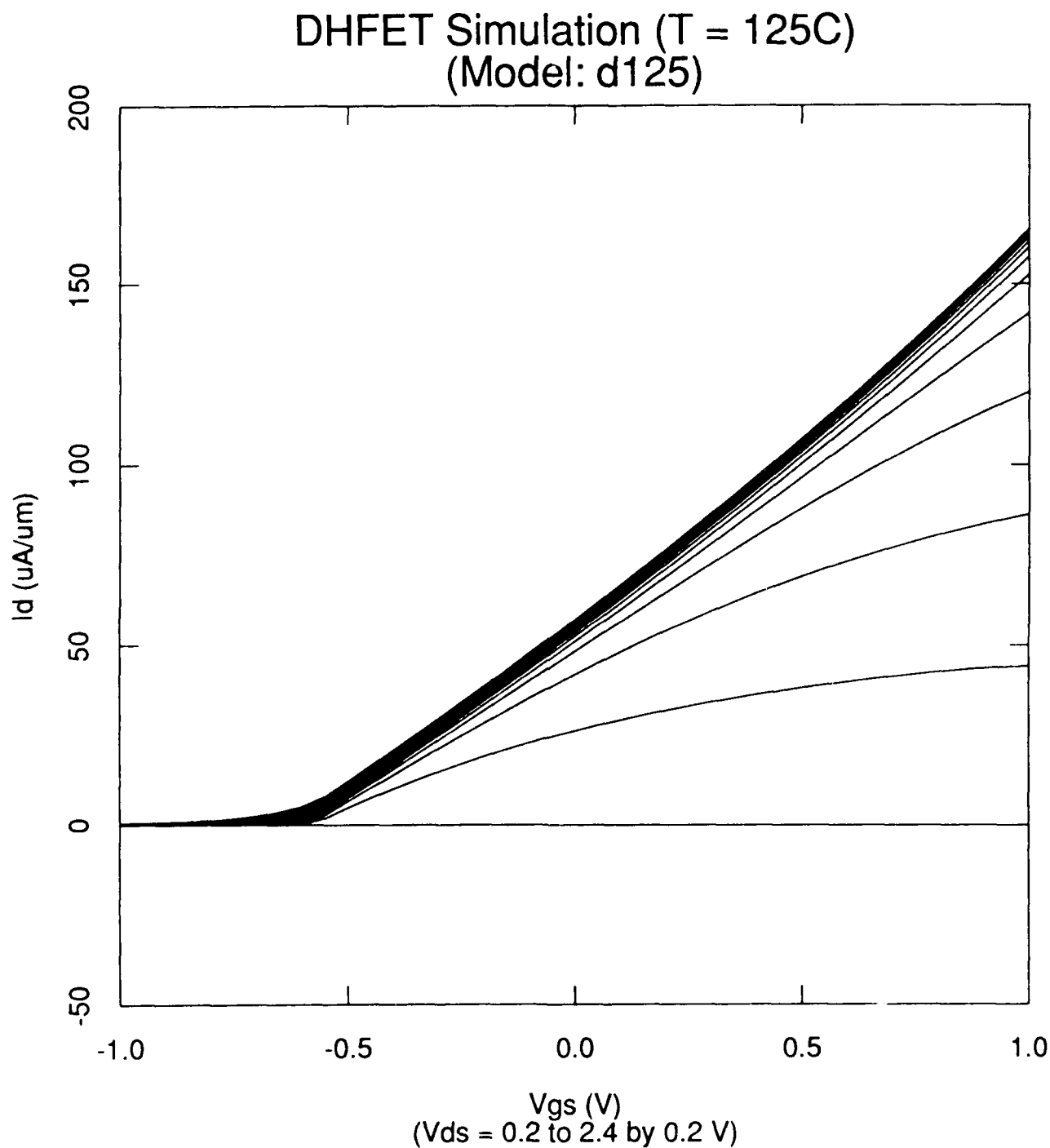


Figure 11. I_d vs. V_{gs} (V_{ds} stepped) for d125 DHFET Simulation at 125C.

DHFET Simulation (T = 125C)
(Model: d125)

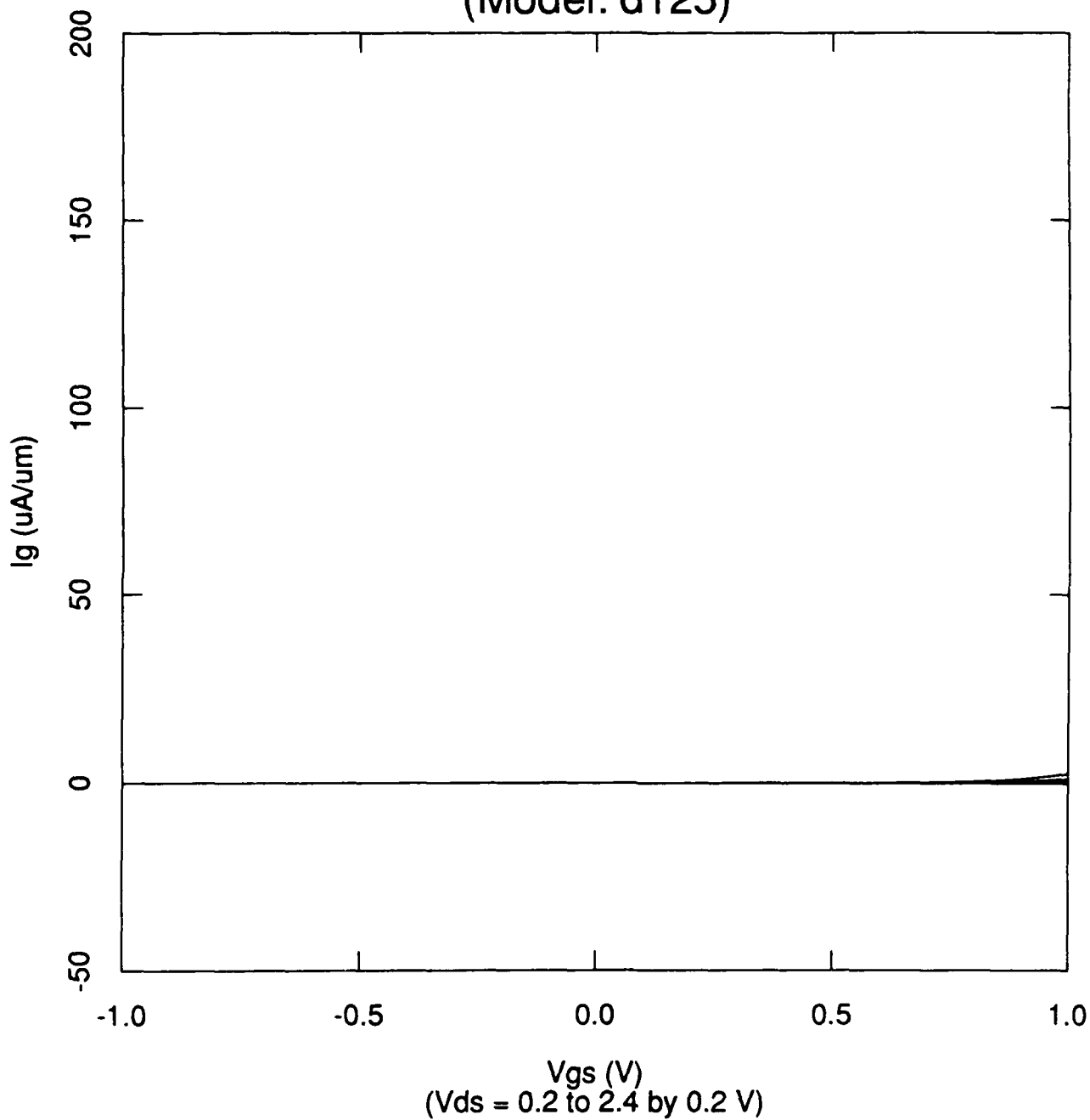


Figure 12. I_g vs. V_{gs} (V_{ds} stepped) for d125 DHFET Simulation at 125C.

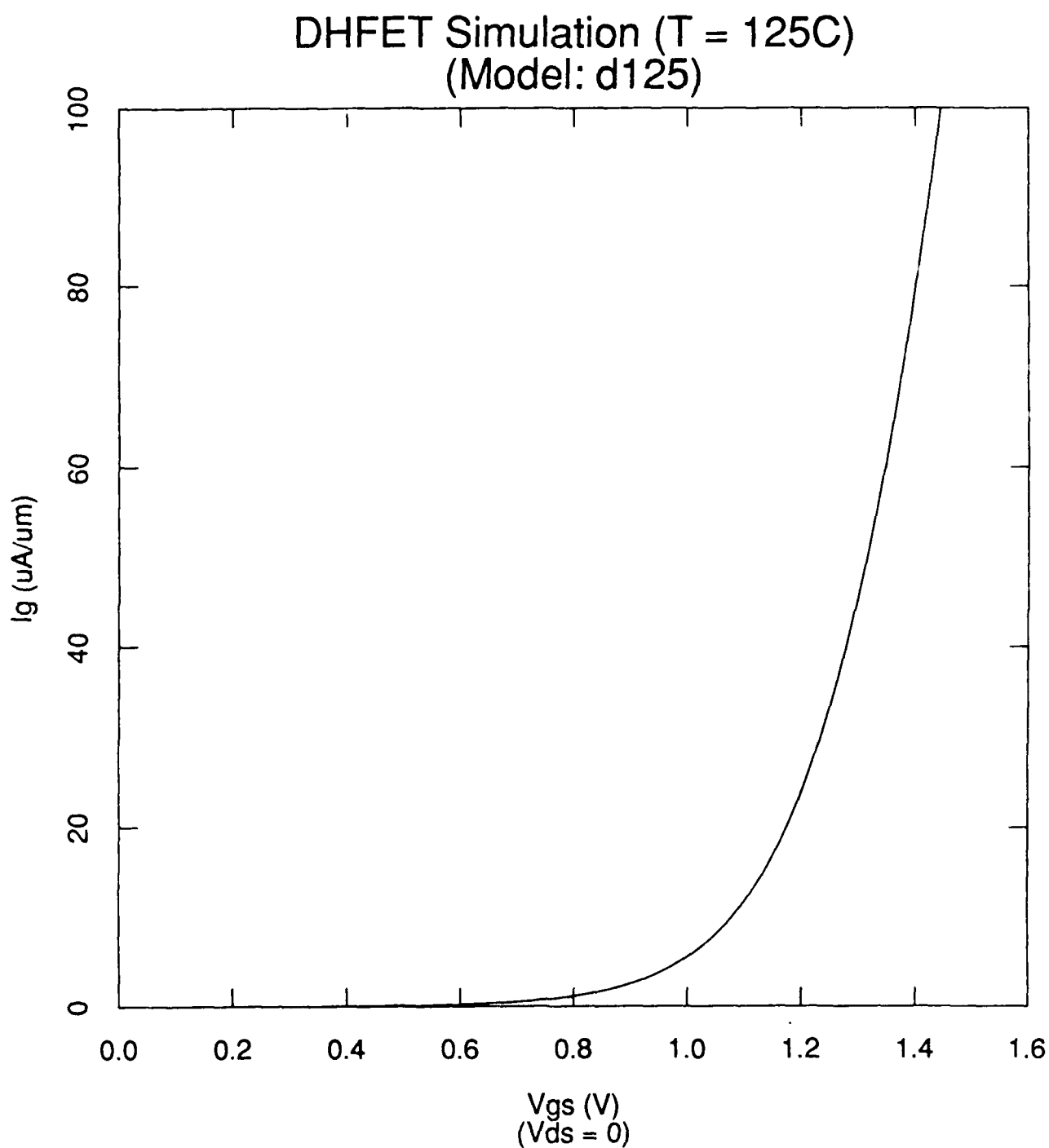


Figure 13. I_g vs. V_{gs} ($V_{ds} = 0$) for d125 DHFET Simulation at 125°C .

DHFET Simulation (T = 125C)
(Model: d125)

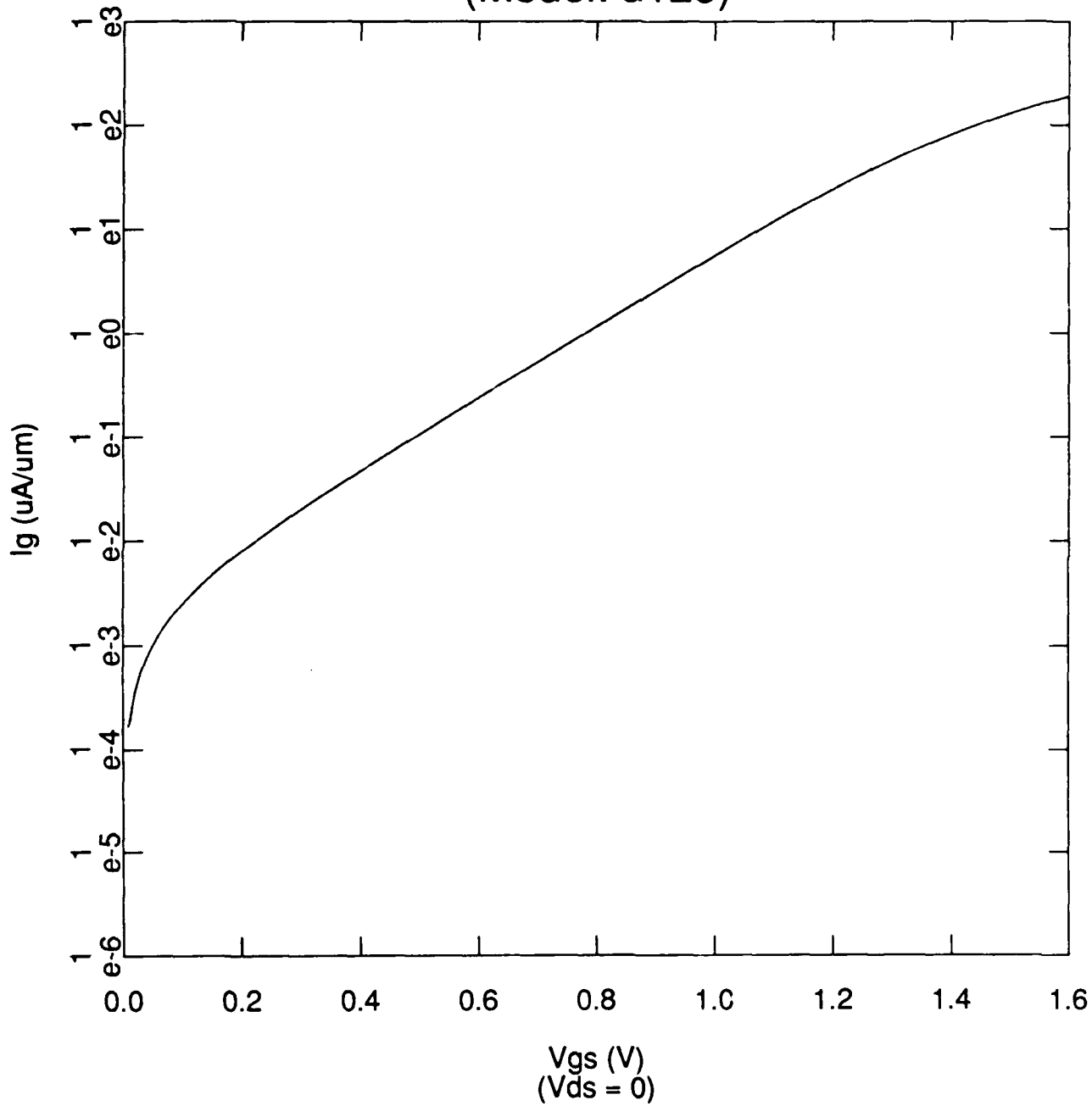


Figure 14. I_g vs. V_{gs} ($V_{ds} = 0$) for d125 DHFET Simulation at 125C (semilog).

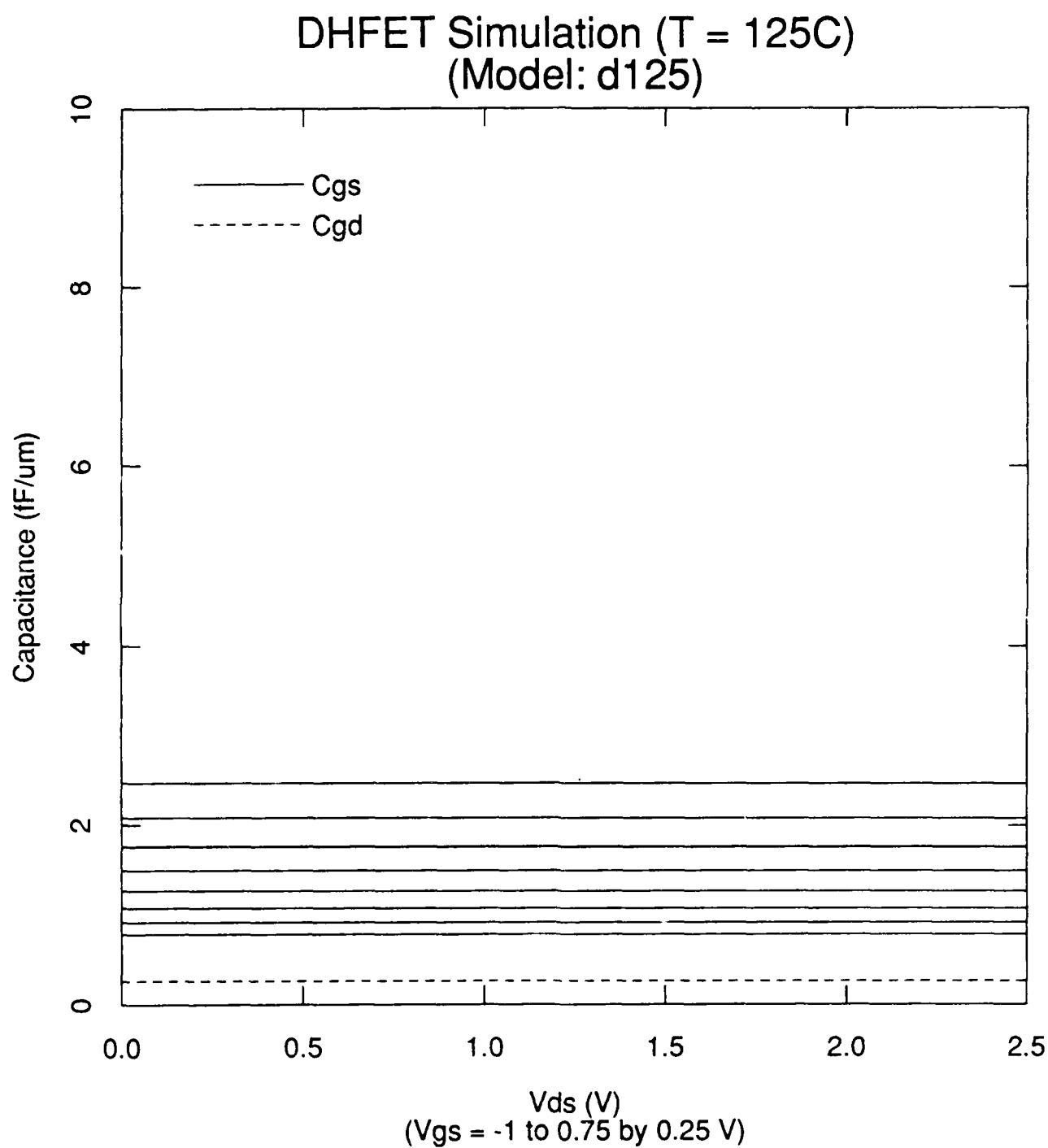


Figure 15. Cgd and Cgs vs. Vds (Vgs stepped) for d125 DHFET Simulation at 125C.

DHFET Simulation (T = 125C) (Model: d125)

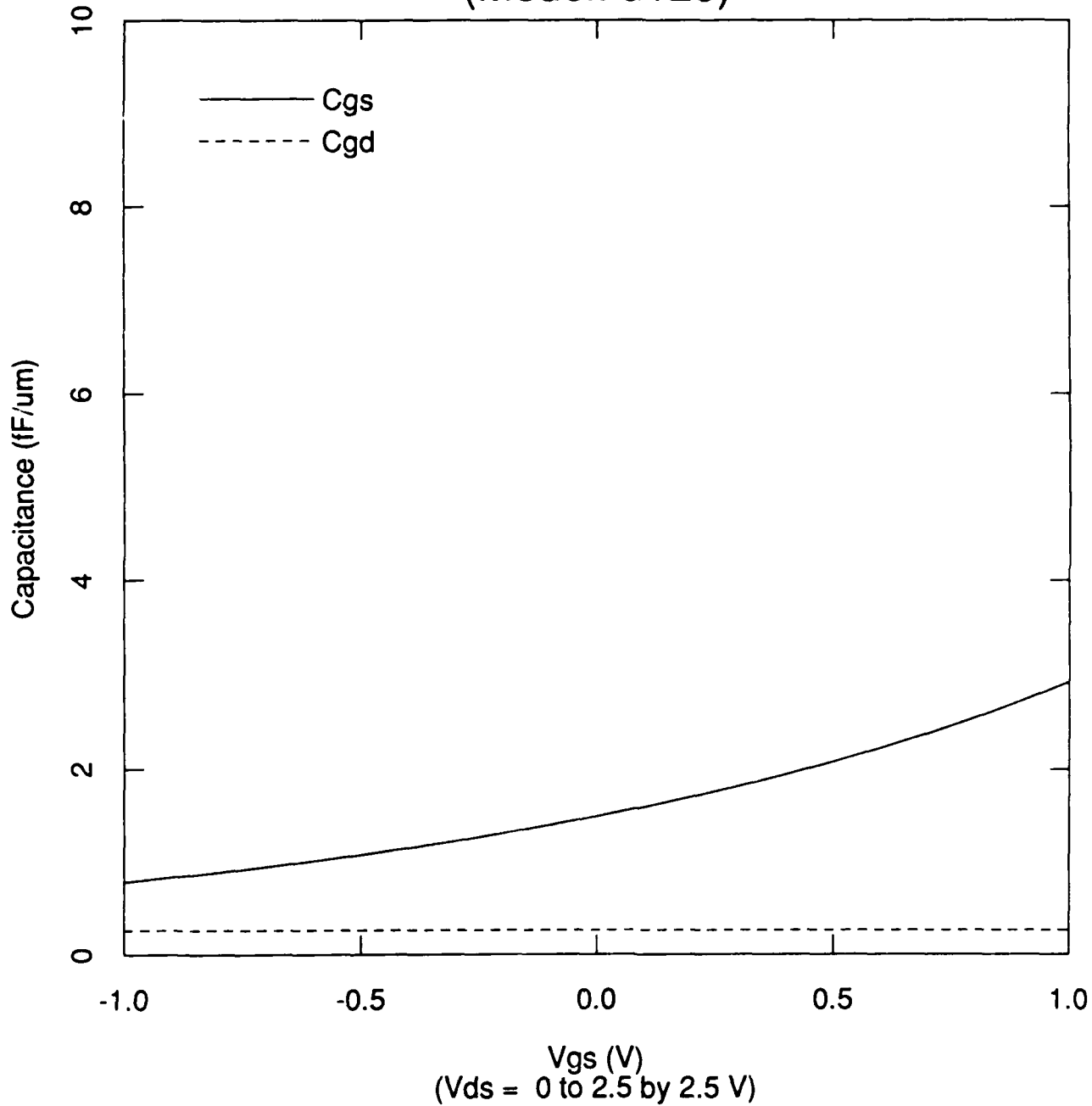


Figure 16. C_{gd} and C_{gs} vs. V_{gs} (V_{ds} stepped) for d125 DHFET Simulation at 125C.

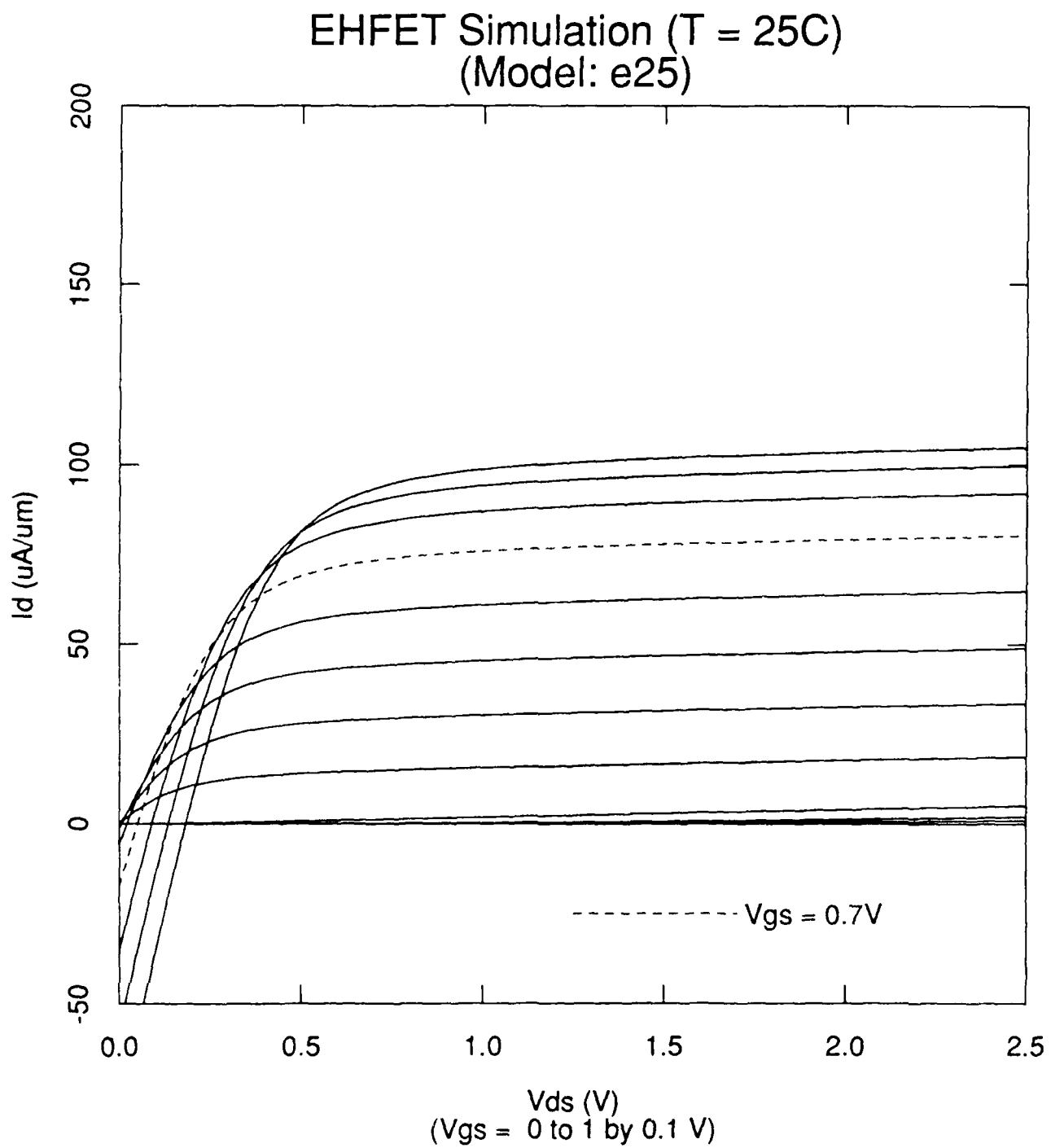


Figure 17. Id vs. Vds (Vgs stepped) for e25 EHFET Simulation at 25C.

EHFET Simulation (T = 25C) (Model: e25)

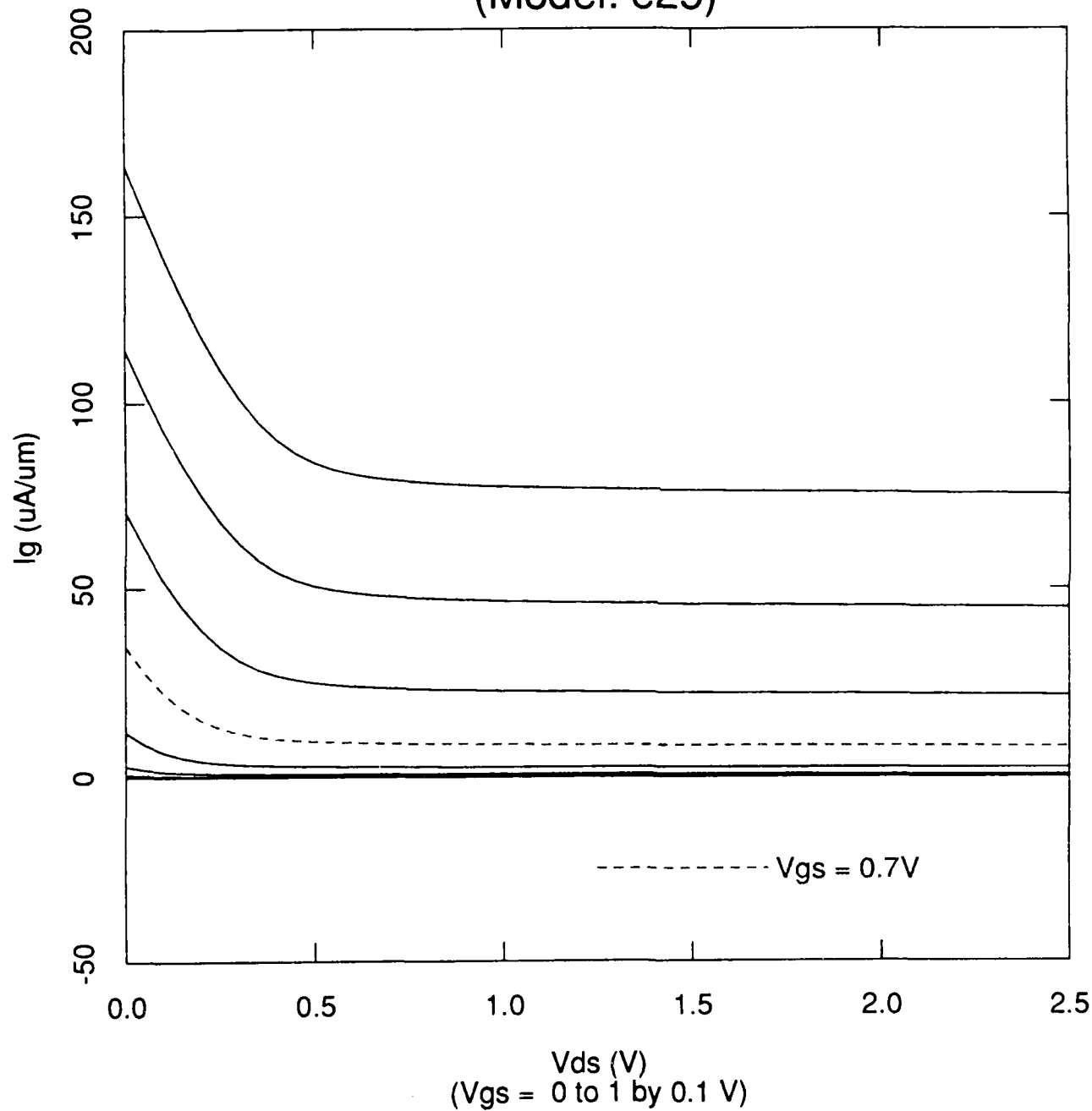


Figure 18. I_g vs. V_{ds} (V_{gs} stepped) for e25 EHFET Simulation at 25C.

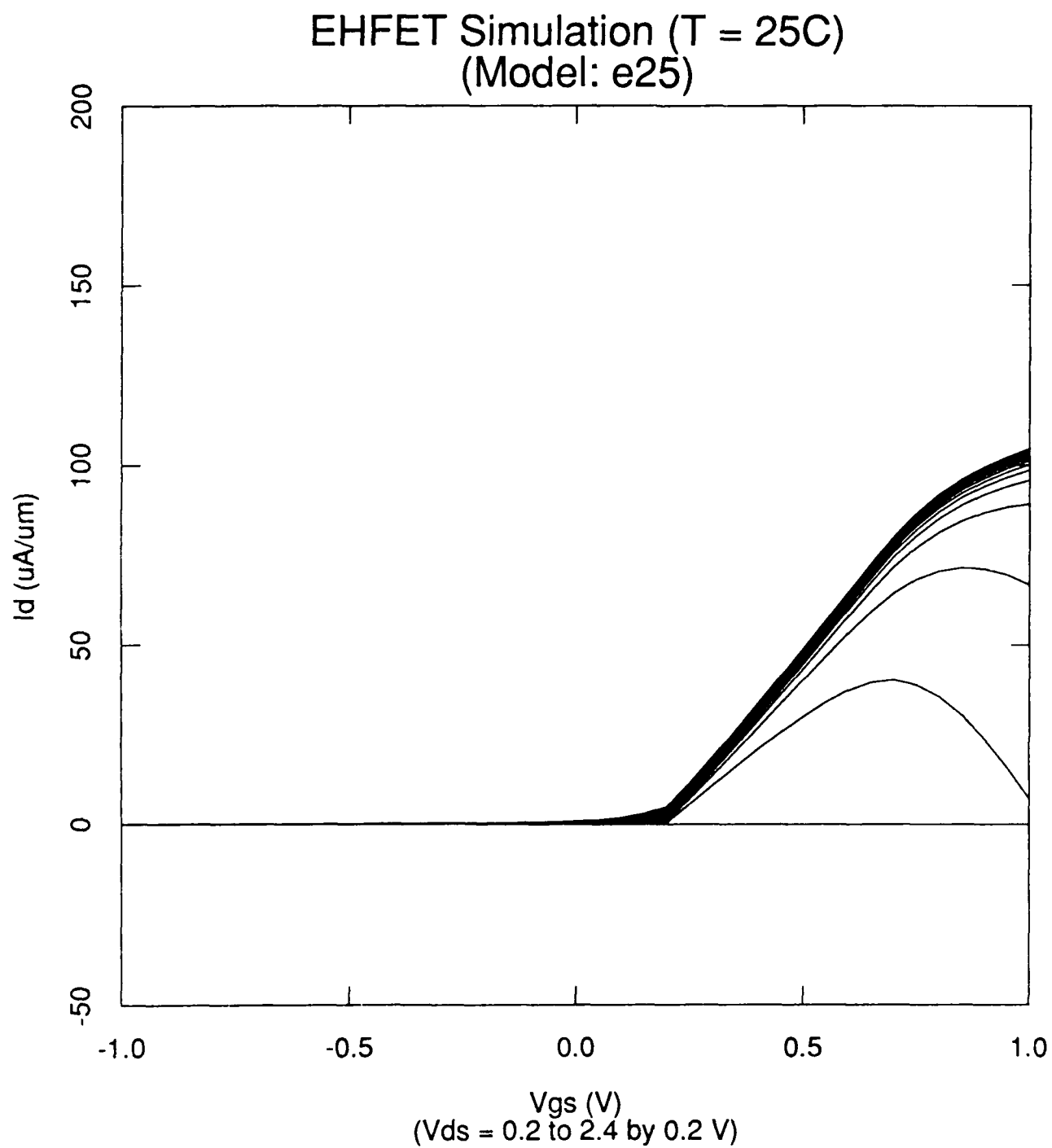


Figure 19. I_d vs. V_{gs} (V_{ds} stepped) for e25 EHFET Simulation at 25C.

EHFET Simulation (T = 25C)
(Model: e25)

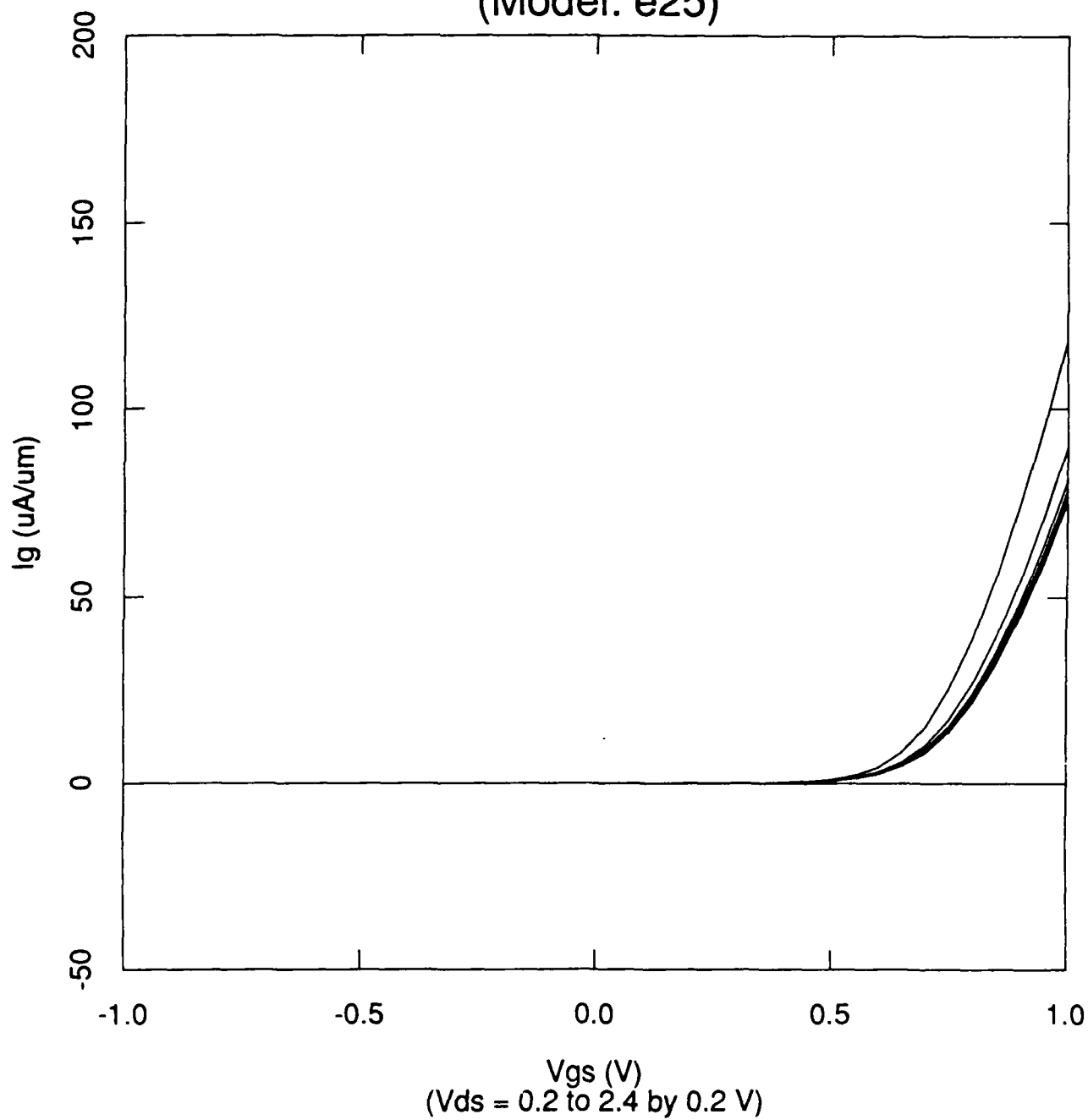


Figure 20. lg vs. Vgs (Vds stepped) for e25 EHFET Simulation at 25C.

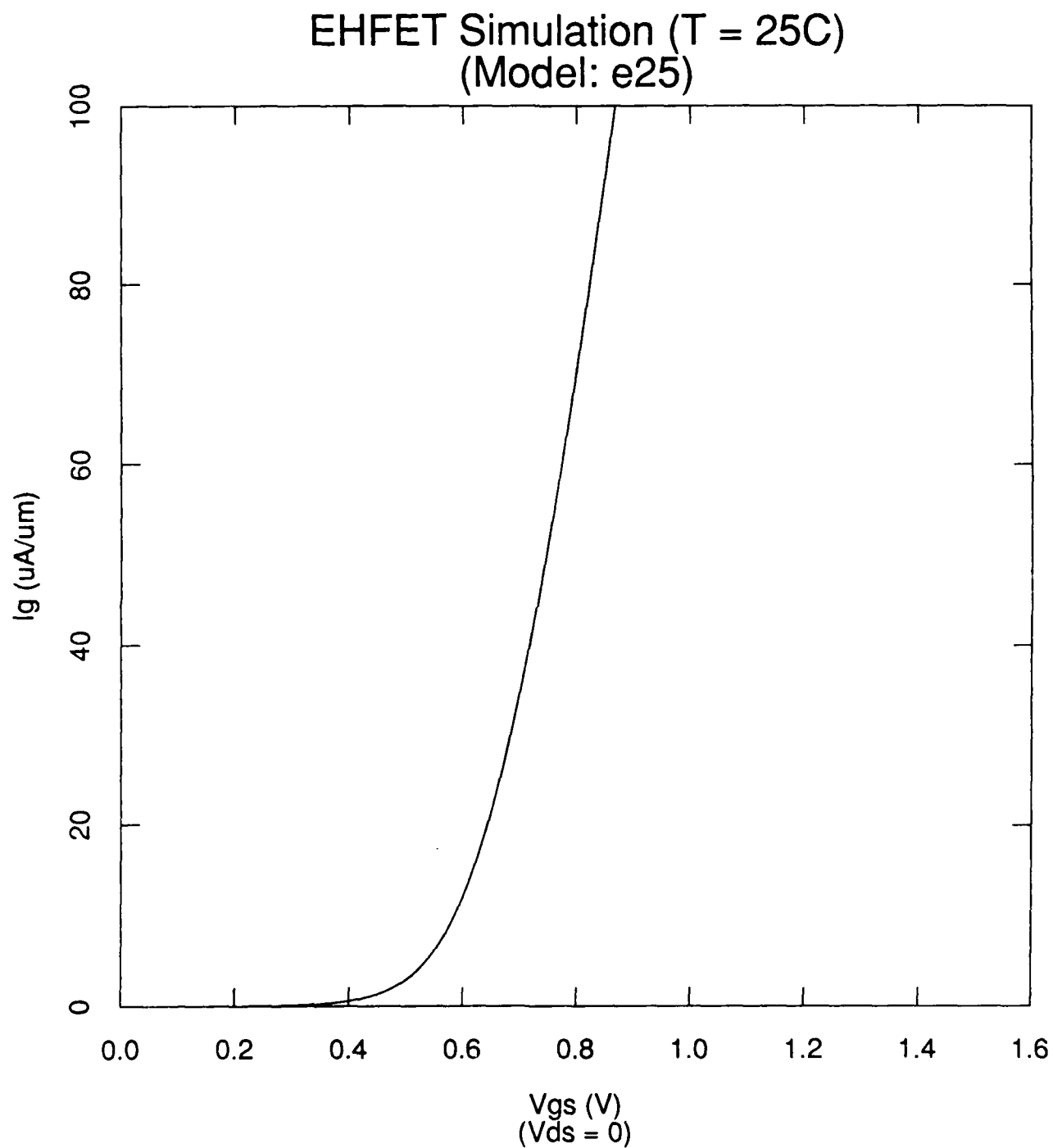


Figure 21. I_g vs. V_{gs} ($V_{ds} = 0$) for e25 EHFET Simulation at 25C.

EHFET Simulation (T = 25C)
(Model: e25)

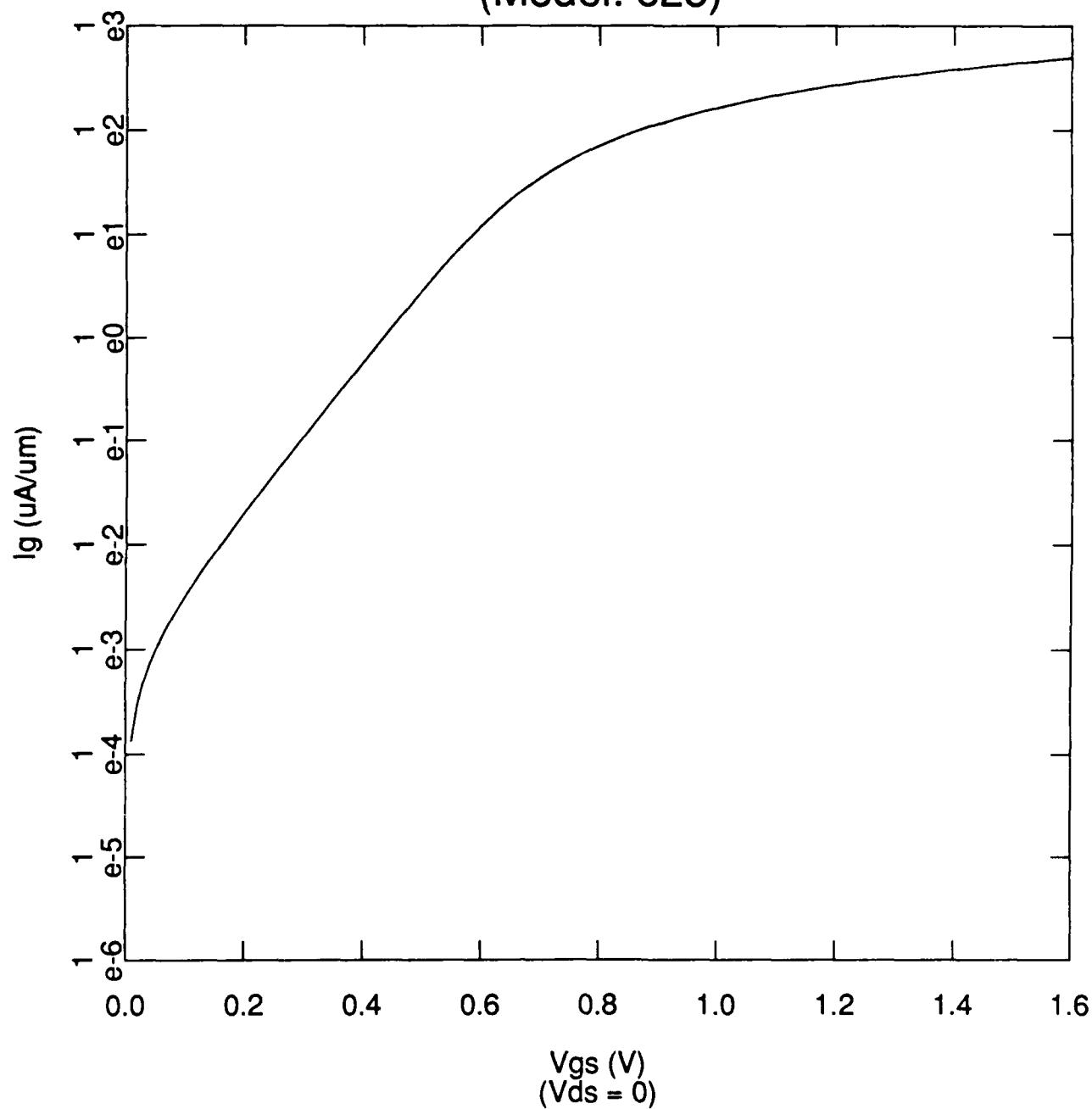


Figure 22. I_g vs. V_{gs} ($V_{ds} = 0$) for e25 EHFET Simulation at 25C (semilog).

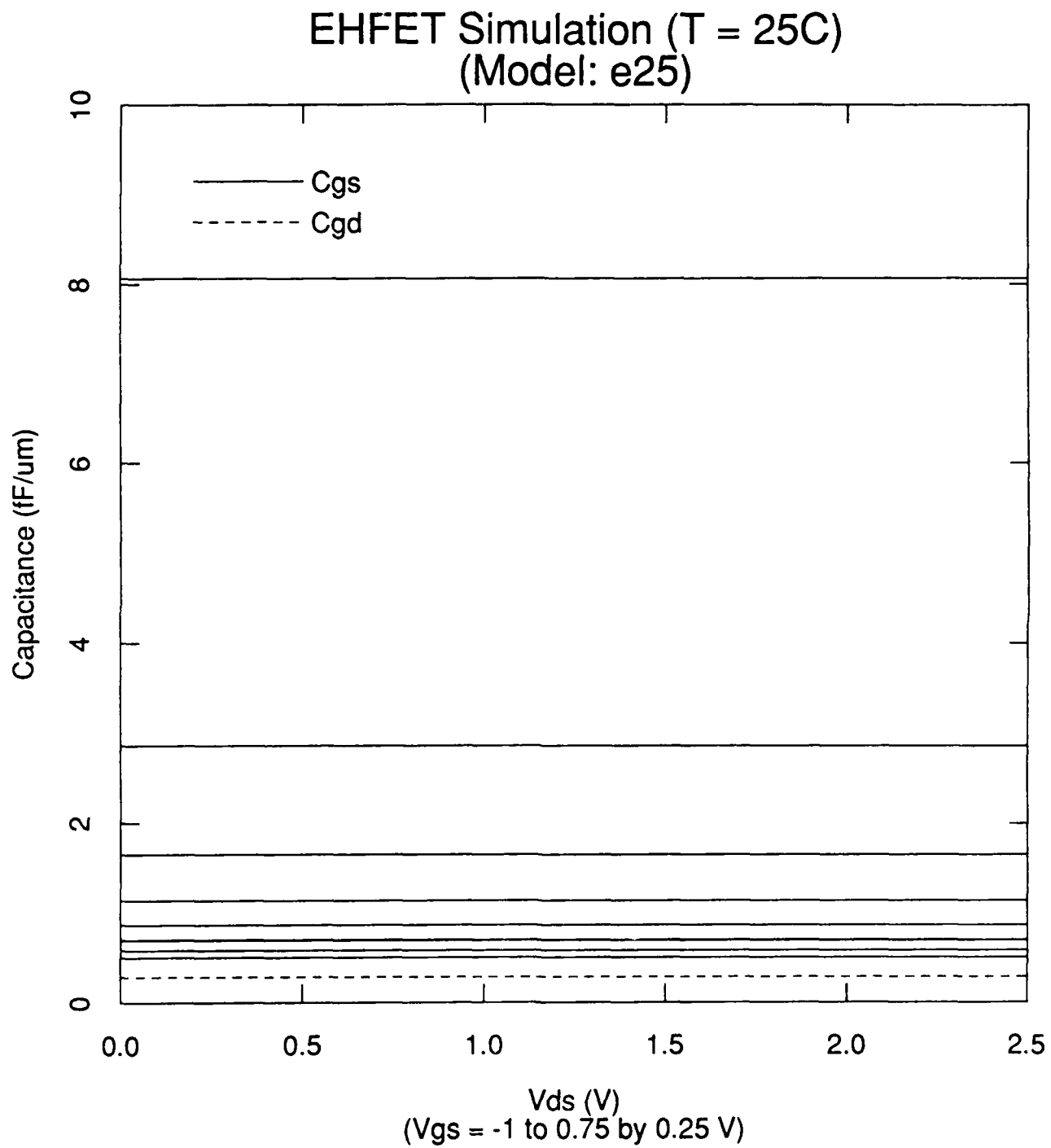


Figure 23. Cgd and Cgs vs. Vds (Vgs stepped) for e25 EHFET Simulation at 25C.

EHFET Simulation (T = 25C)
(Model: e25)

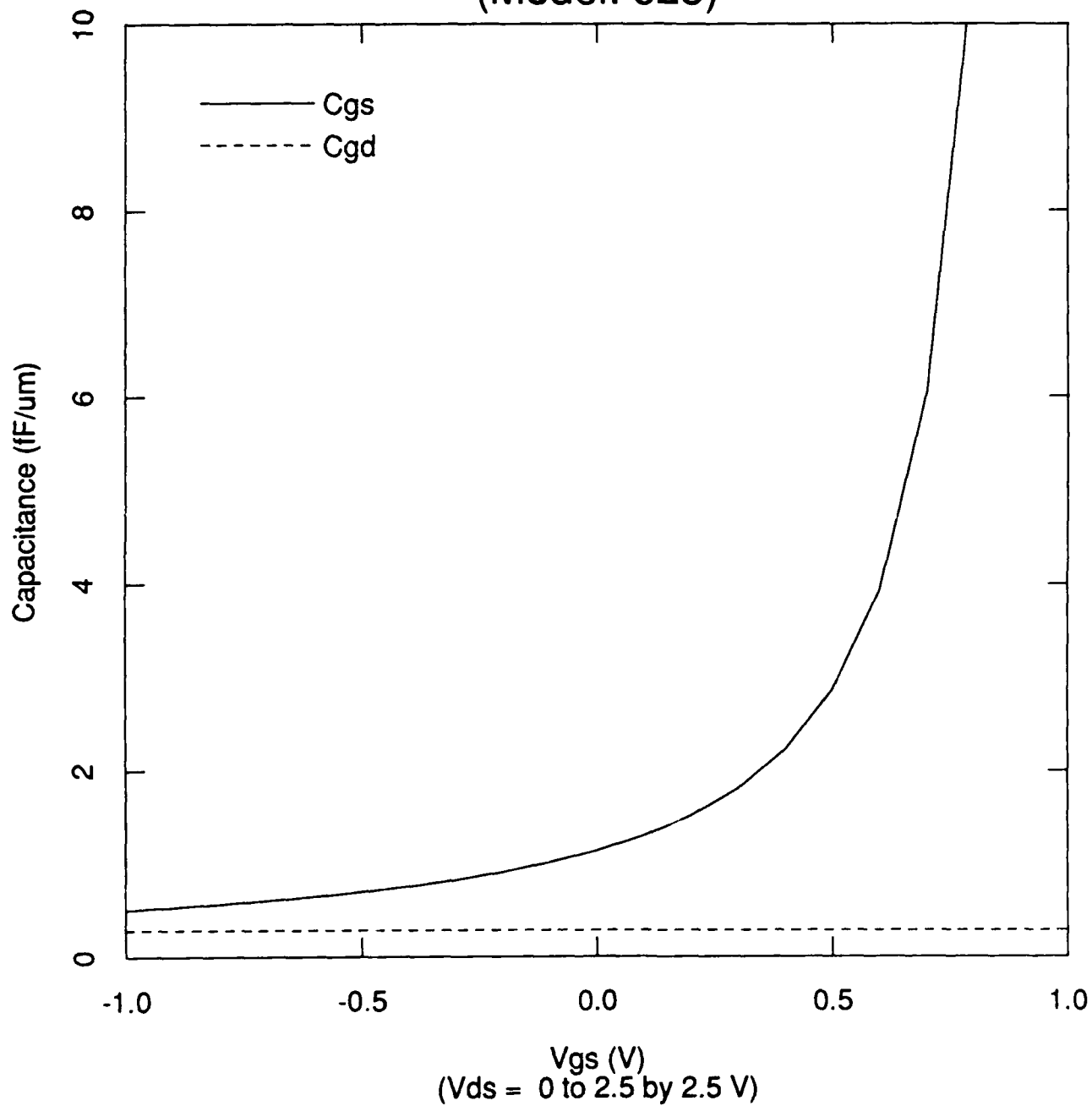


Figure 24. Cgd and Cgs vs. Vgs (Vds stepped) for e25 EHFET Simulation at 25C.

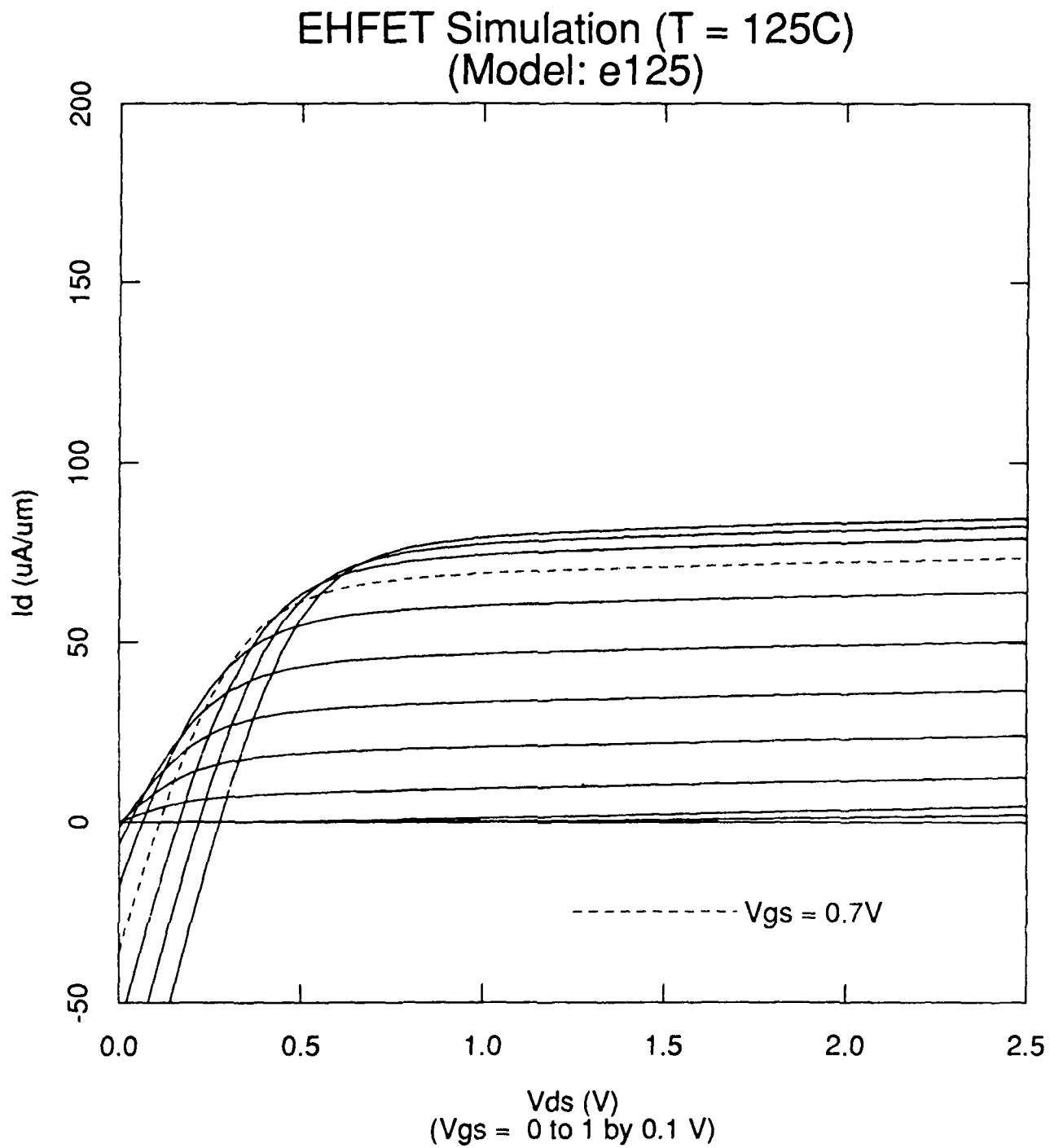


Figure 25. I_d vs. V_{ds} (V_{gs} stepped) for e125 EHFET Simulation at 125C.

EHFET Simulation (T = 125C) (Model: e125)

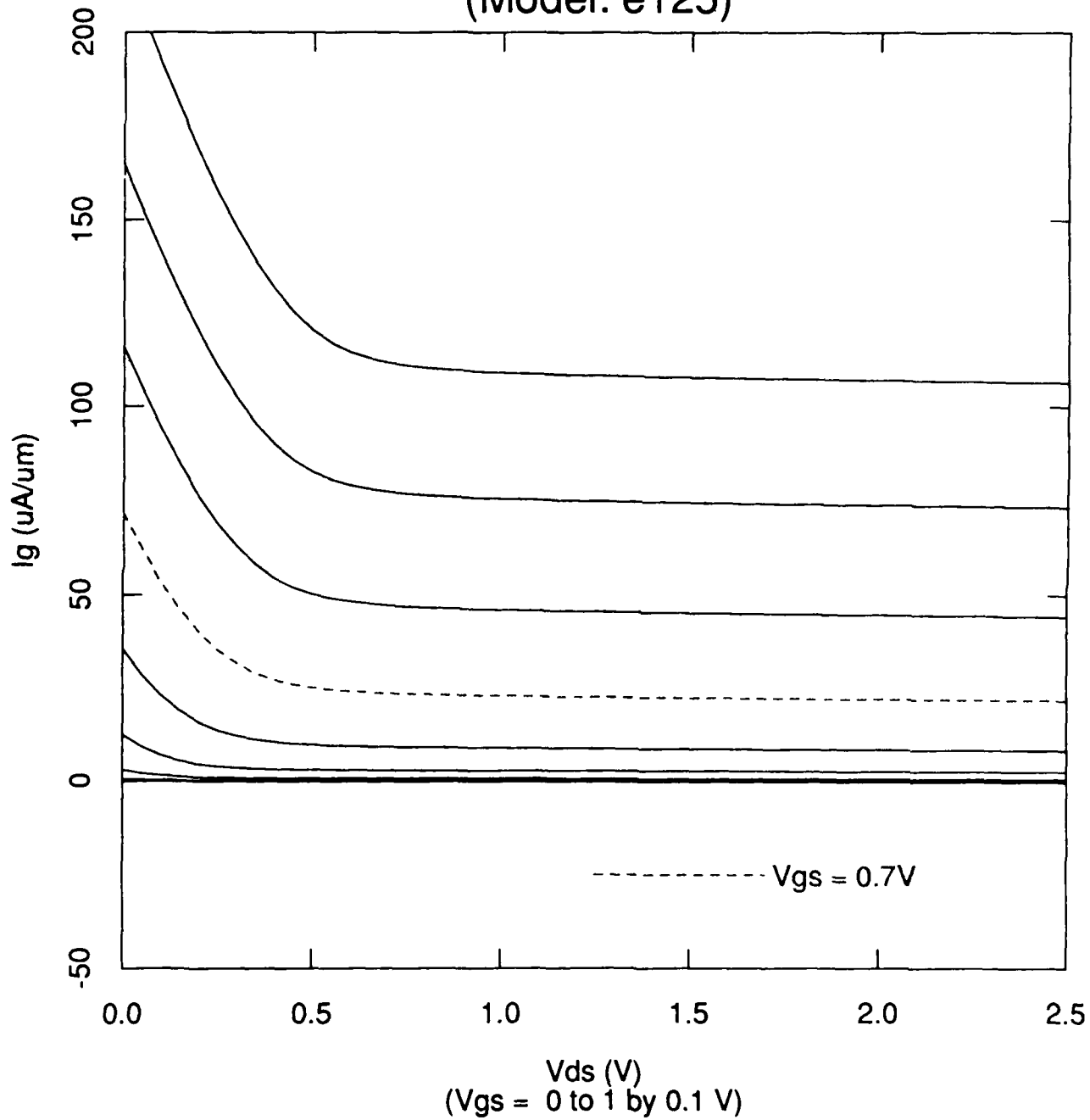


Figure 26. I_g vs. V_{ds} (V_{gs} stepped) for e125 EHFET Simulation at 125C.

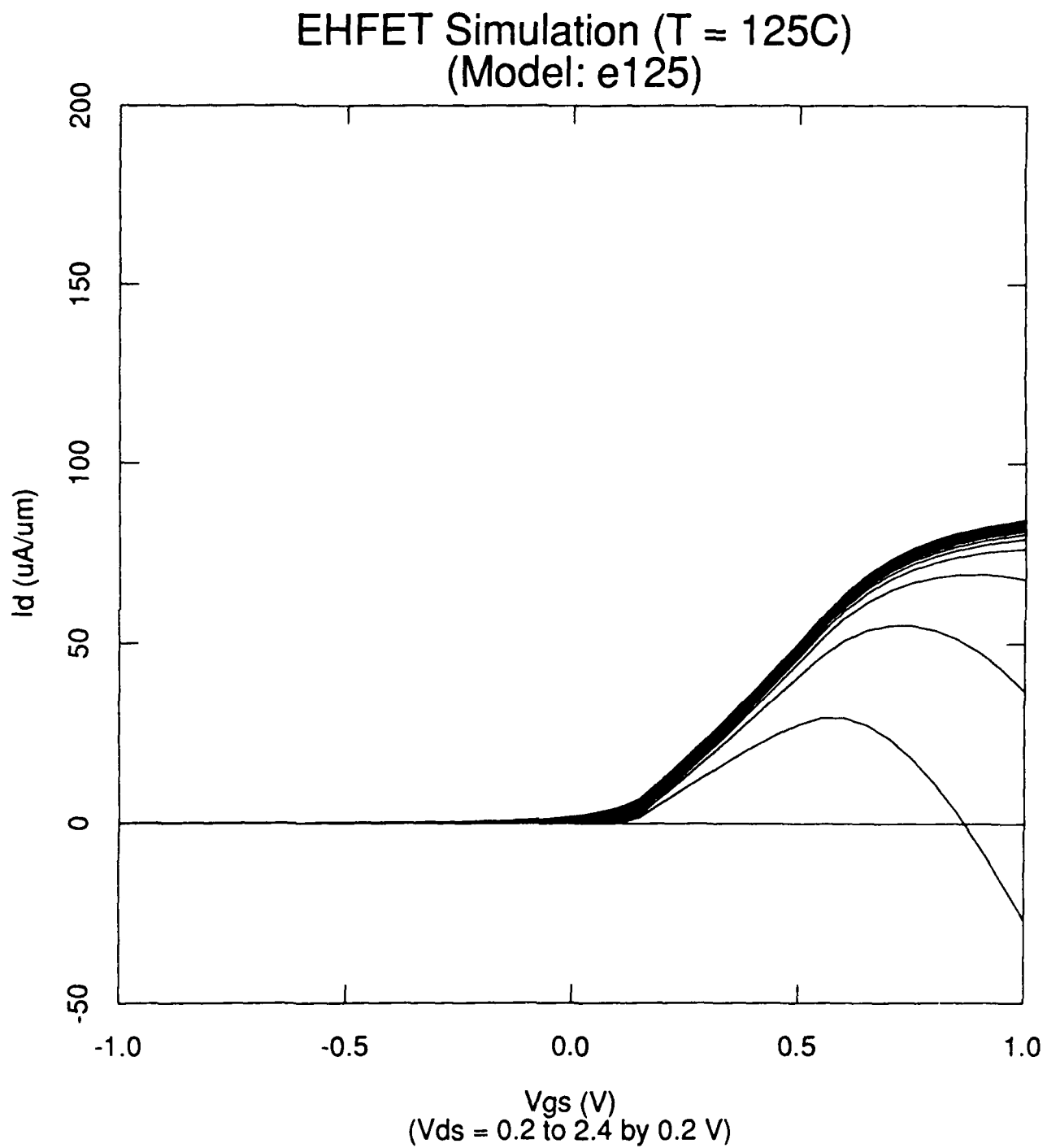


Figure 27. I_d vs. V_{gs} (V_{ds} stepped) for e125 EHFET Simulation at 125°C .

EHFET Simulation (T = 125C)
(Model: e125)

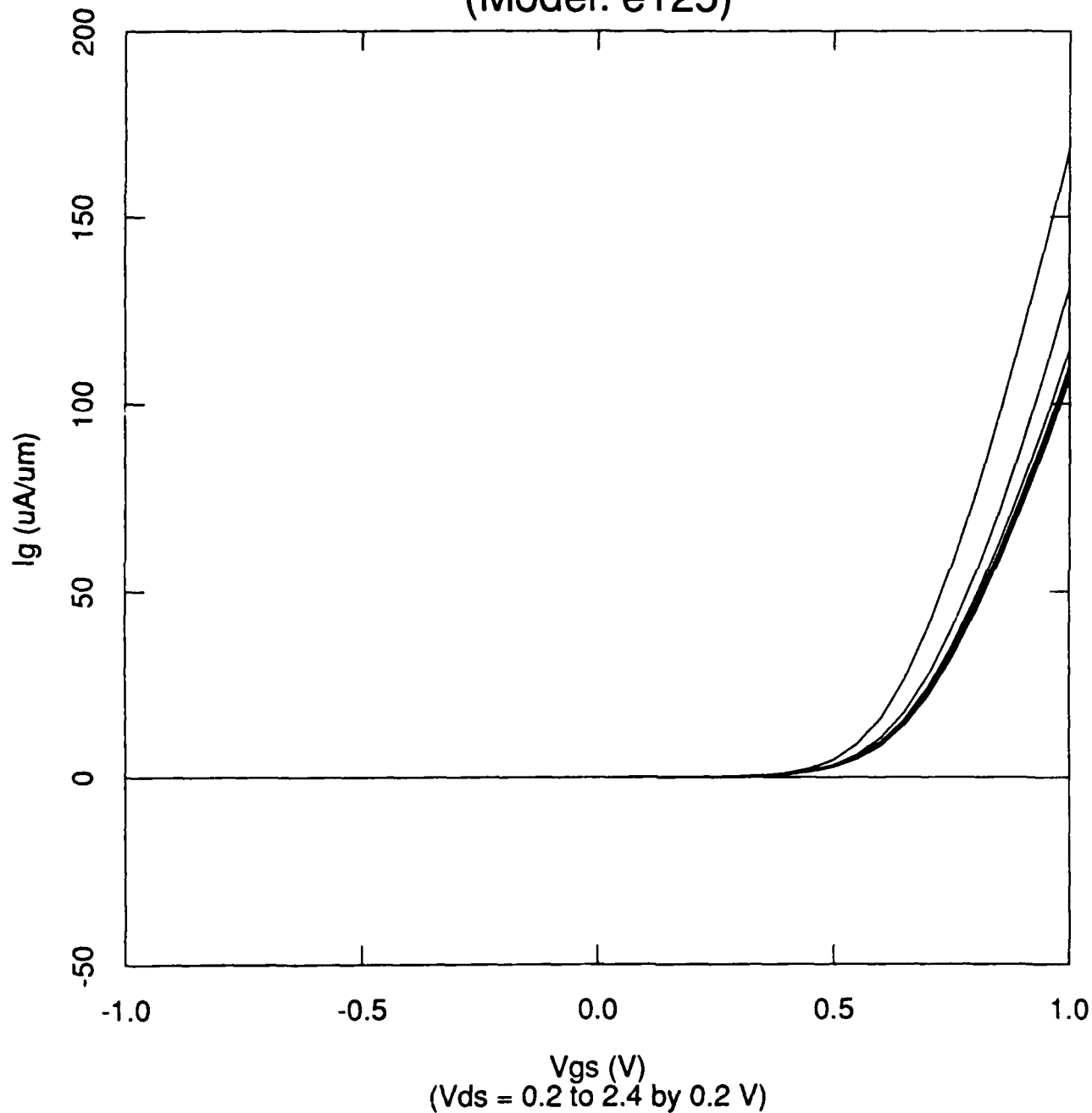


Figure 28. I_g vs. V_{gs} (V_{ds} stepped) for e125 EHFET Simulation at 125C.

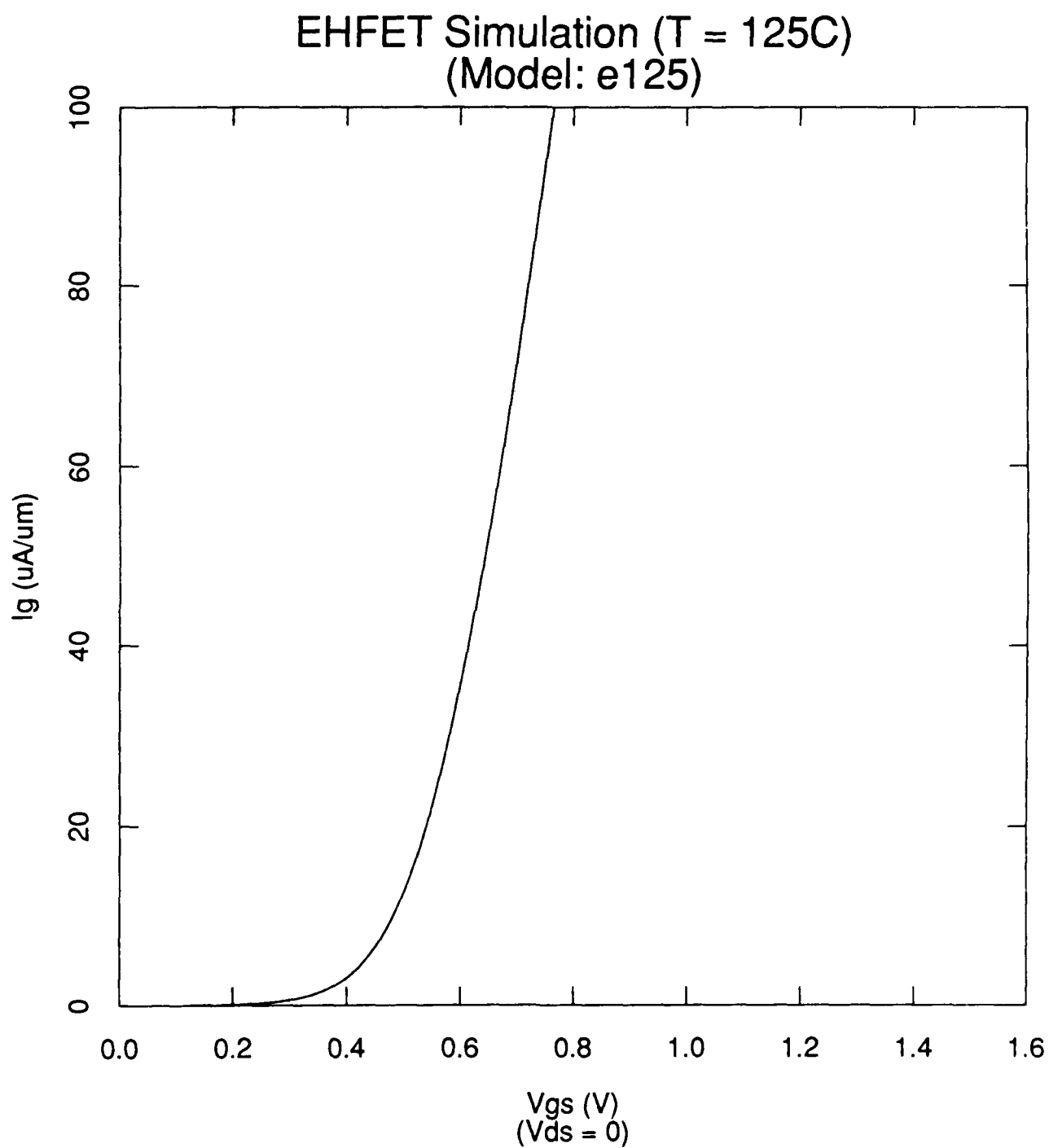


Figure 29. \lg vs. V_{gs} ($V_{ds} = 0$) for e125 EHFET Simulation at 125C.

EHFET Simulation (T = 125C)
(Model: e125)

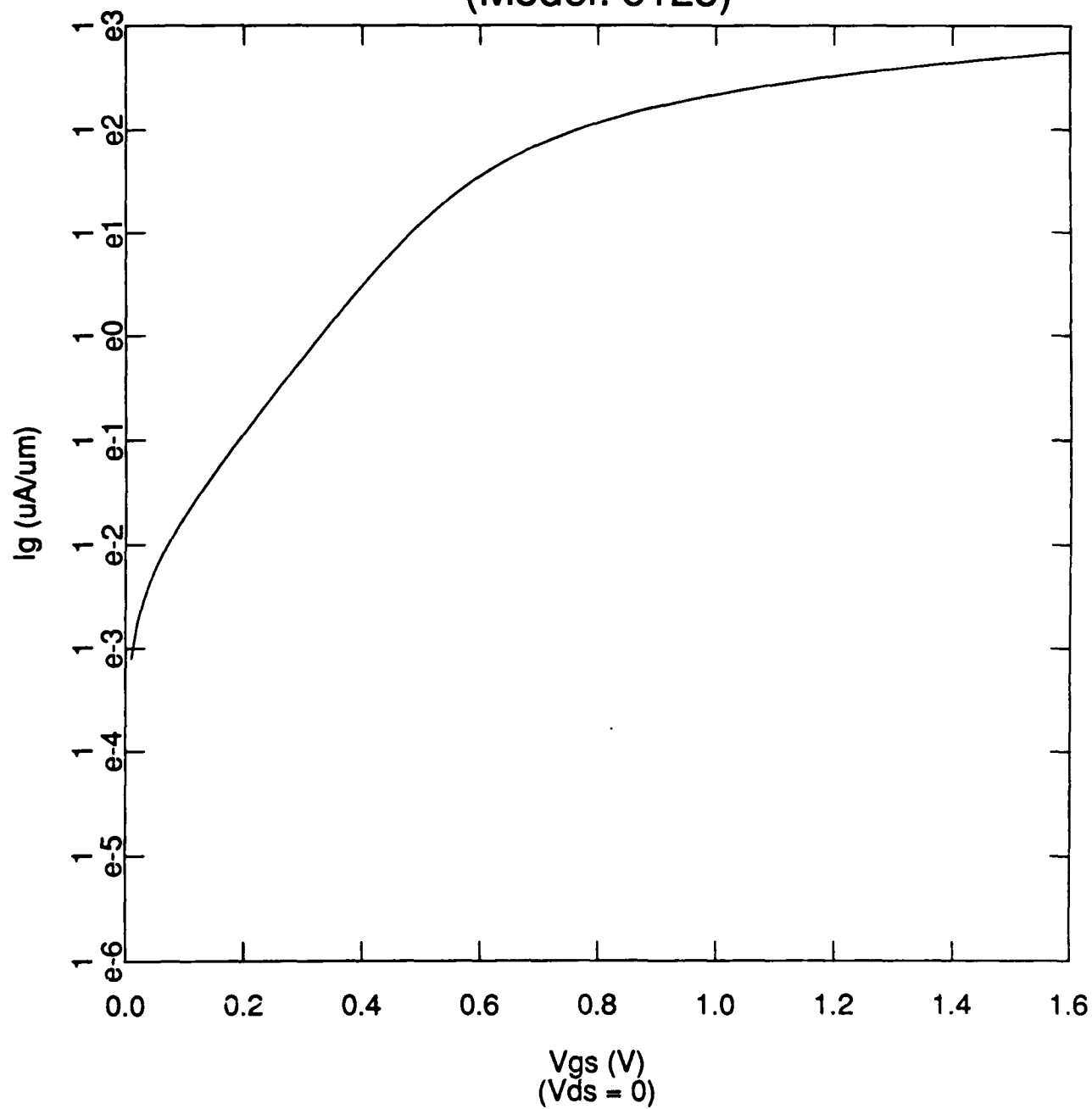


Figure 30. I_g vs. V_{gs} ($V_{ds} = 0$) for e125 EHFET Simulation at 125C (semilog).

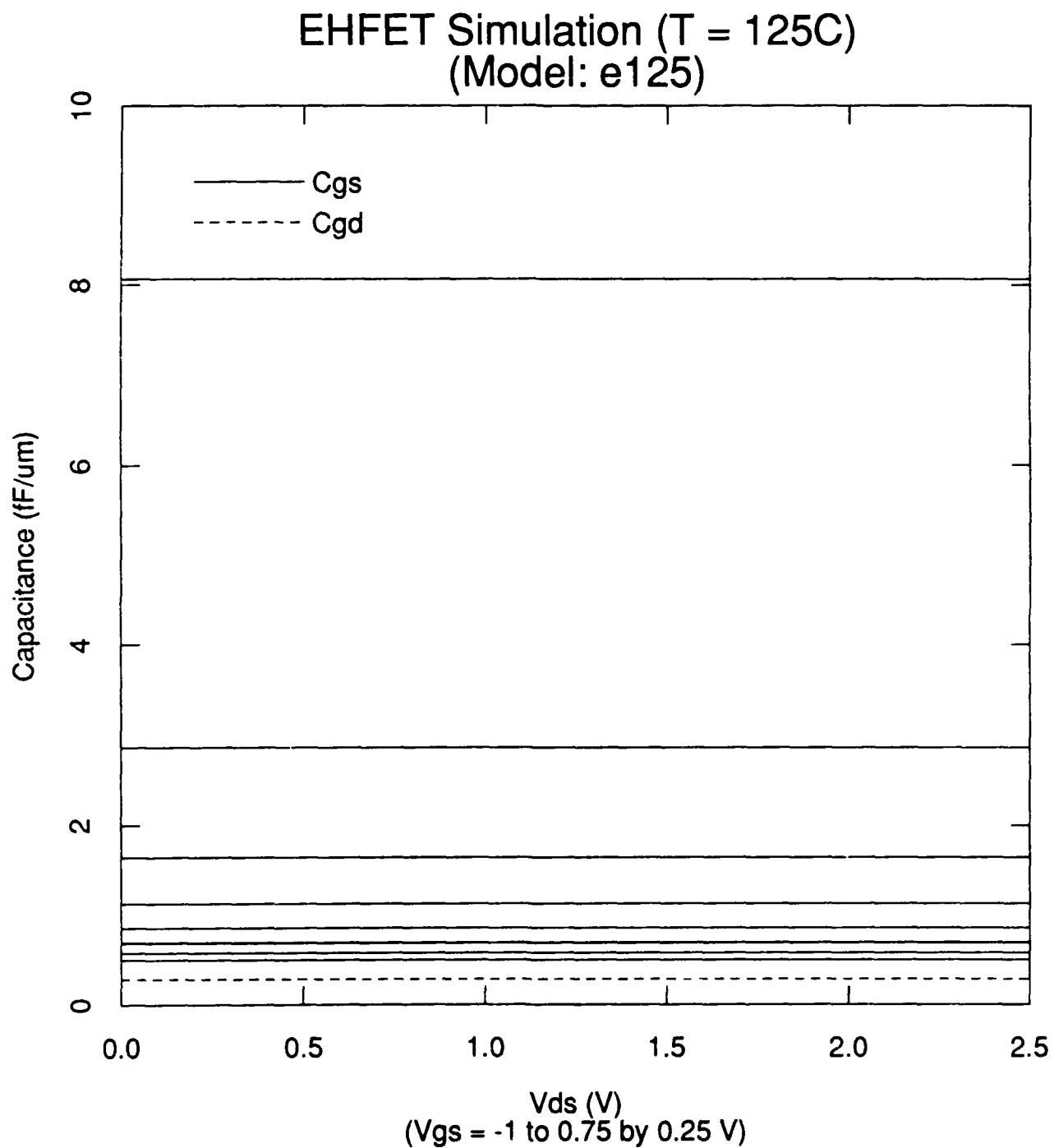


Figure 31. Cgd and Cgs vs. Vds (Vgs stepped) for e125 EHFET Simulation at 125C.

EHFET Simulation (T = 125C)
(Model: e125)

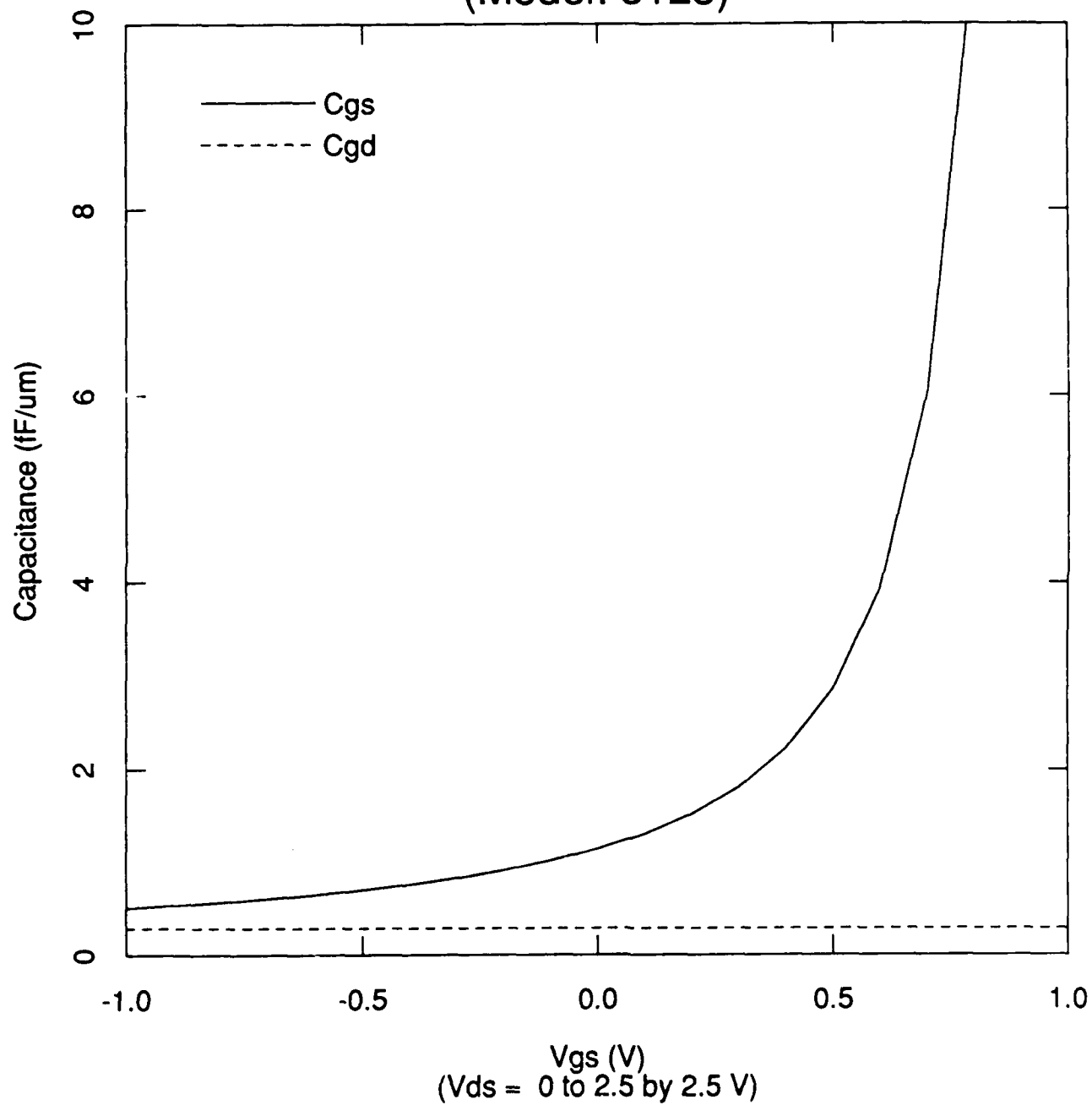


Figure 32. Cgd and Cgs vs. Vgs (Vds stepped) for e125 EHFET Simulation at 125C.

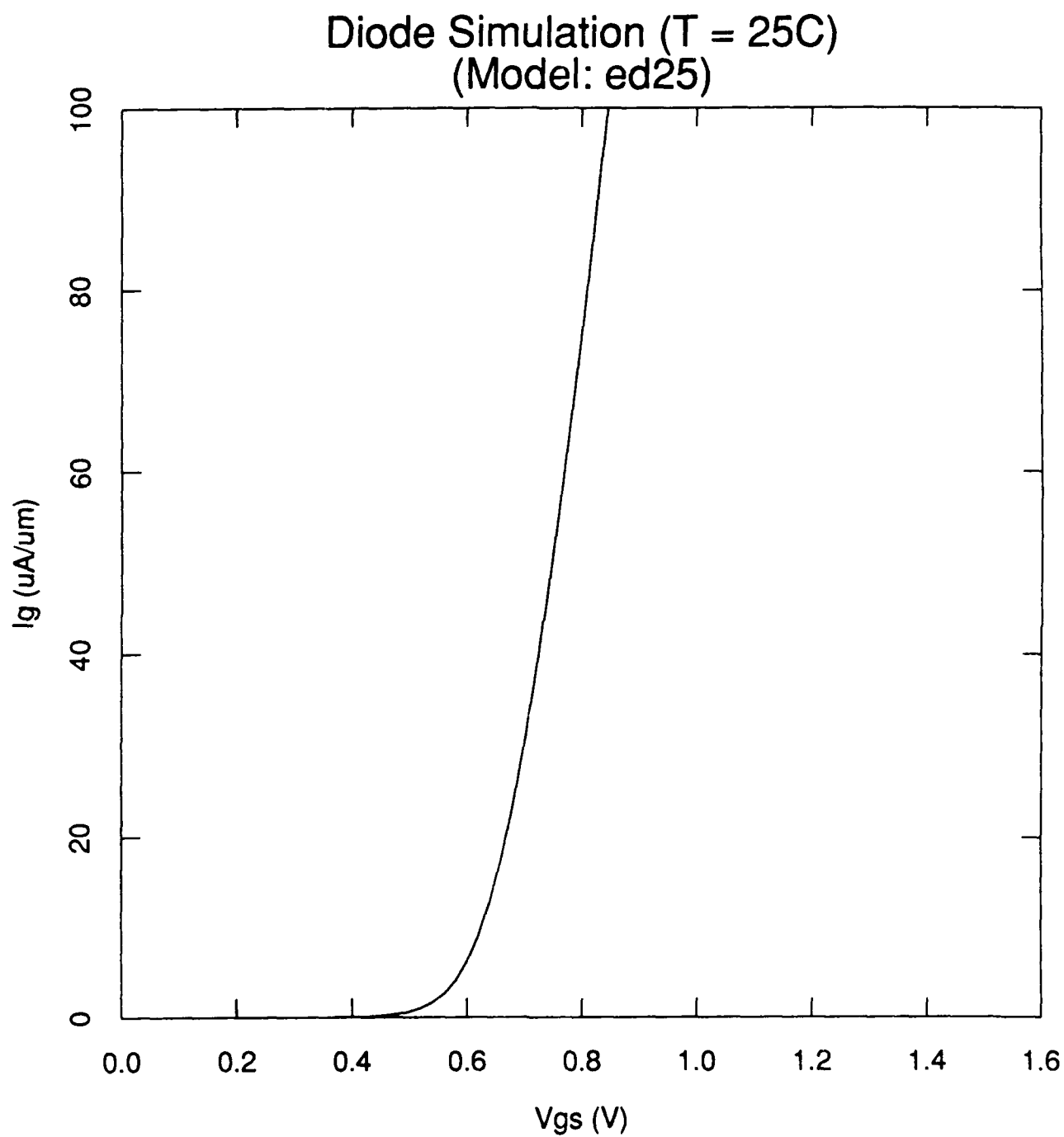


Figure 33. I_g vs. V_{gs} for ed25 Diode Simulation at 25C.

Diode Simulation (T = 25C)
(Model: ed25)

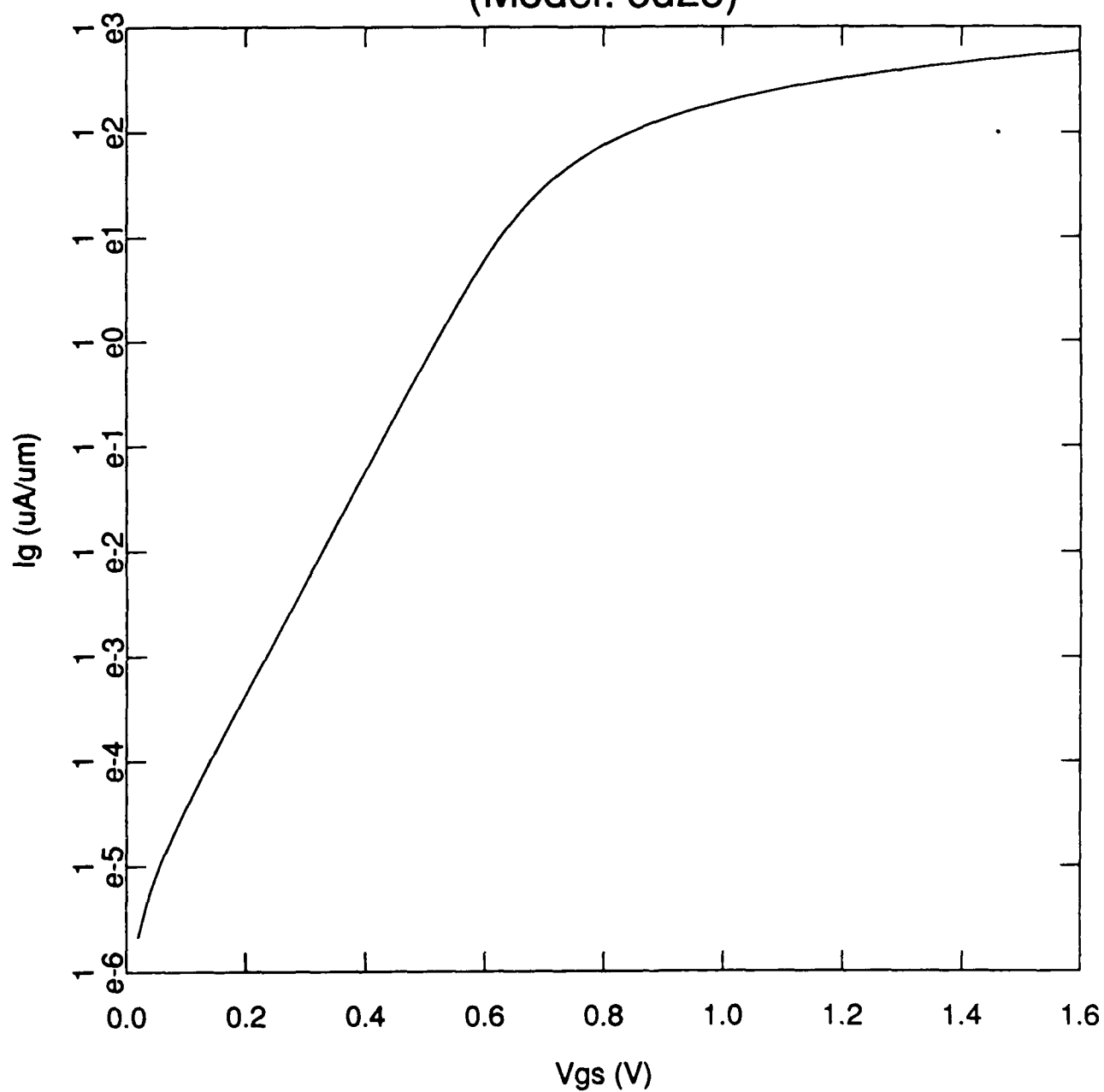


Figure 34. I_g vs. V_{gs} for ed25 Diode Simulation at 25C (semilog).

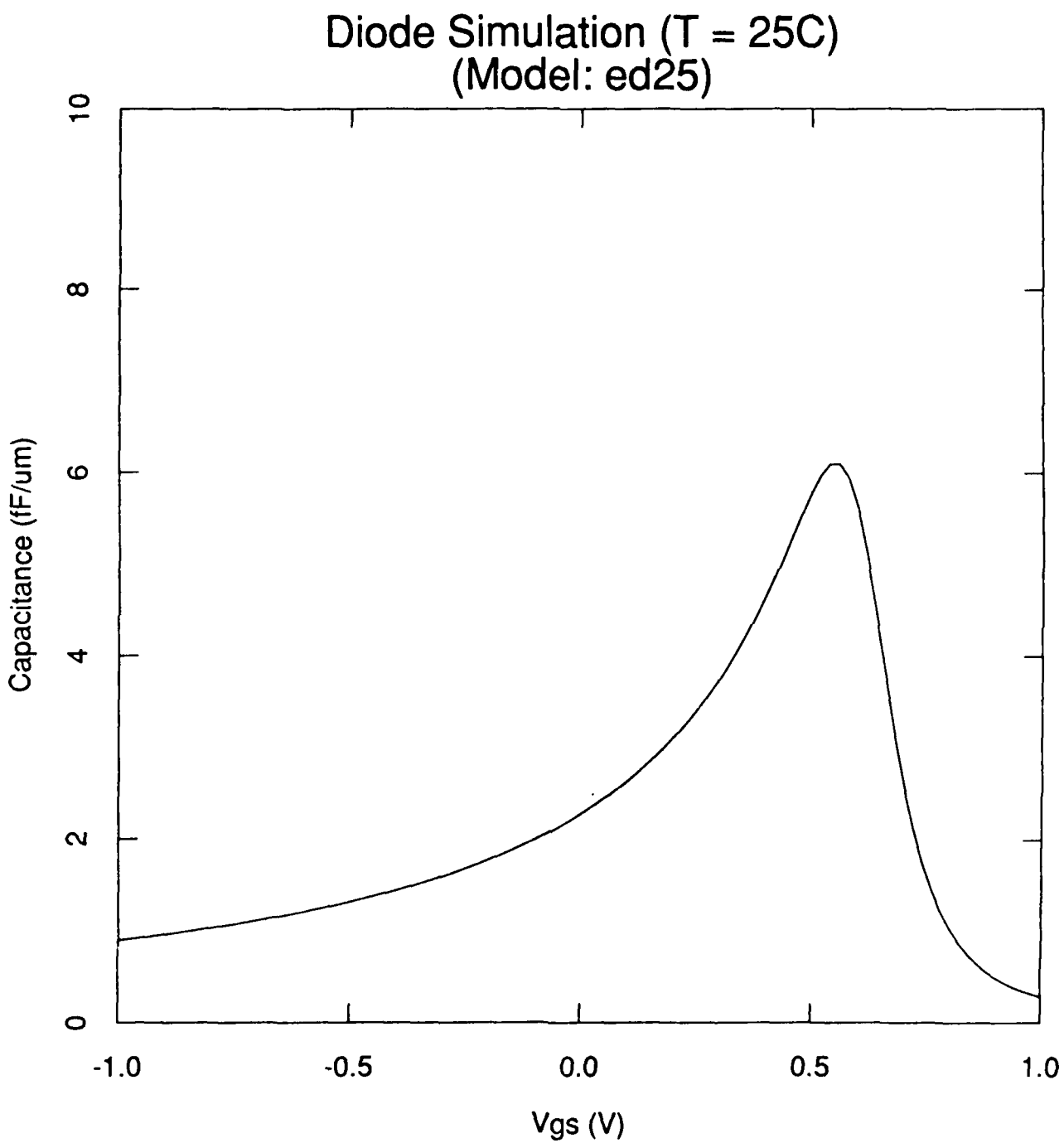


Figure 35. C vs. V_{ds} for ed25 Diode Simulation at 25C.

Diode Simulation (T = 125C)
(Model: ed125)

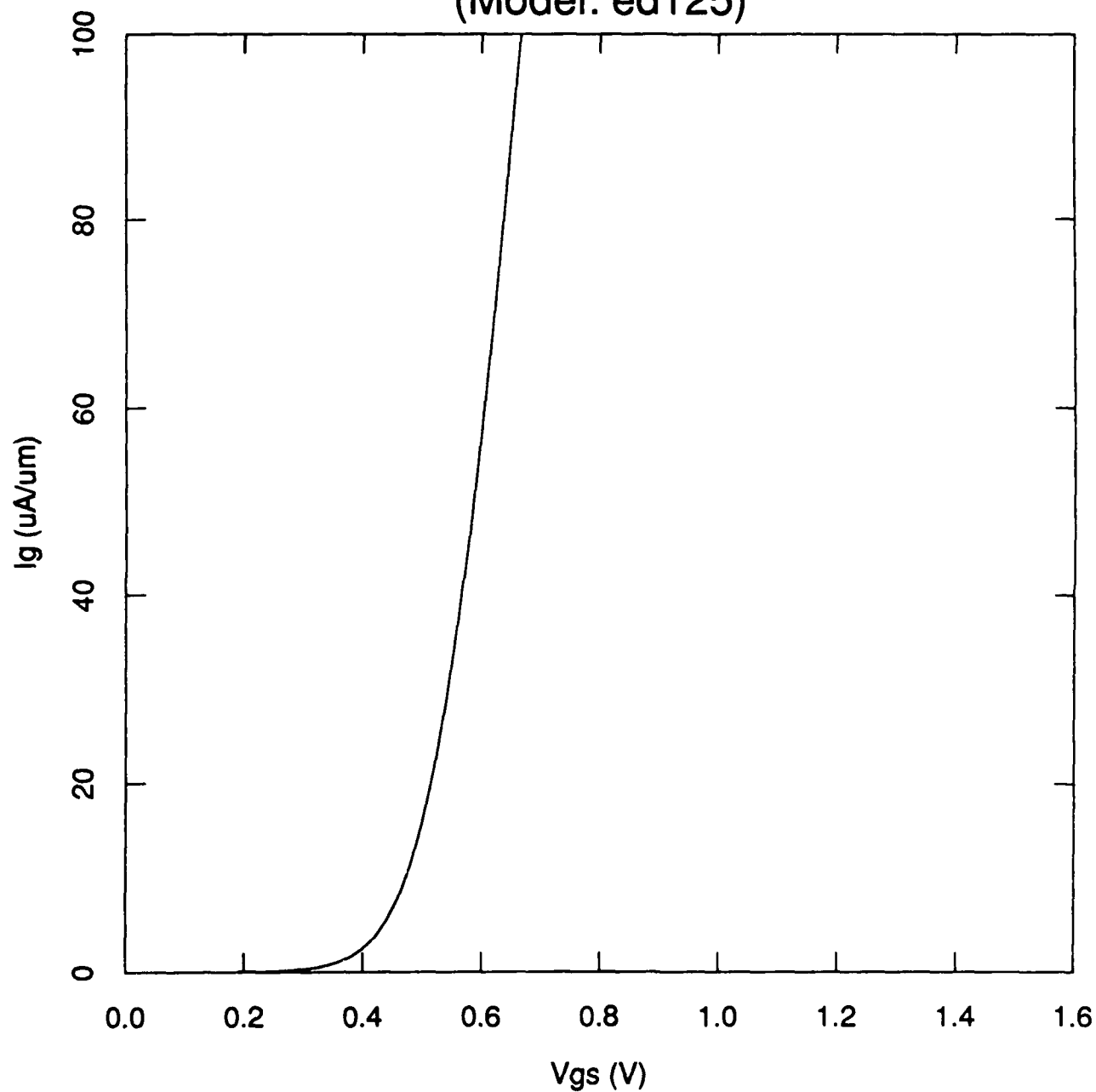


Figure 36. I_g vs. V_{gs} for ed125 Diode Simulation at 125C.

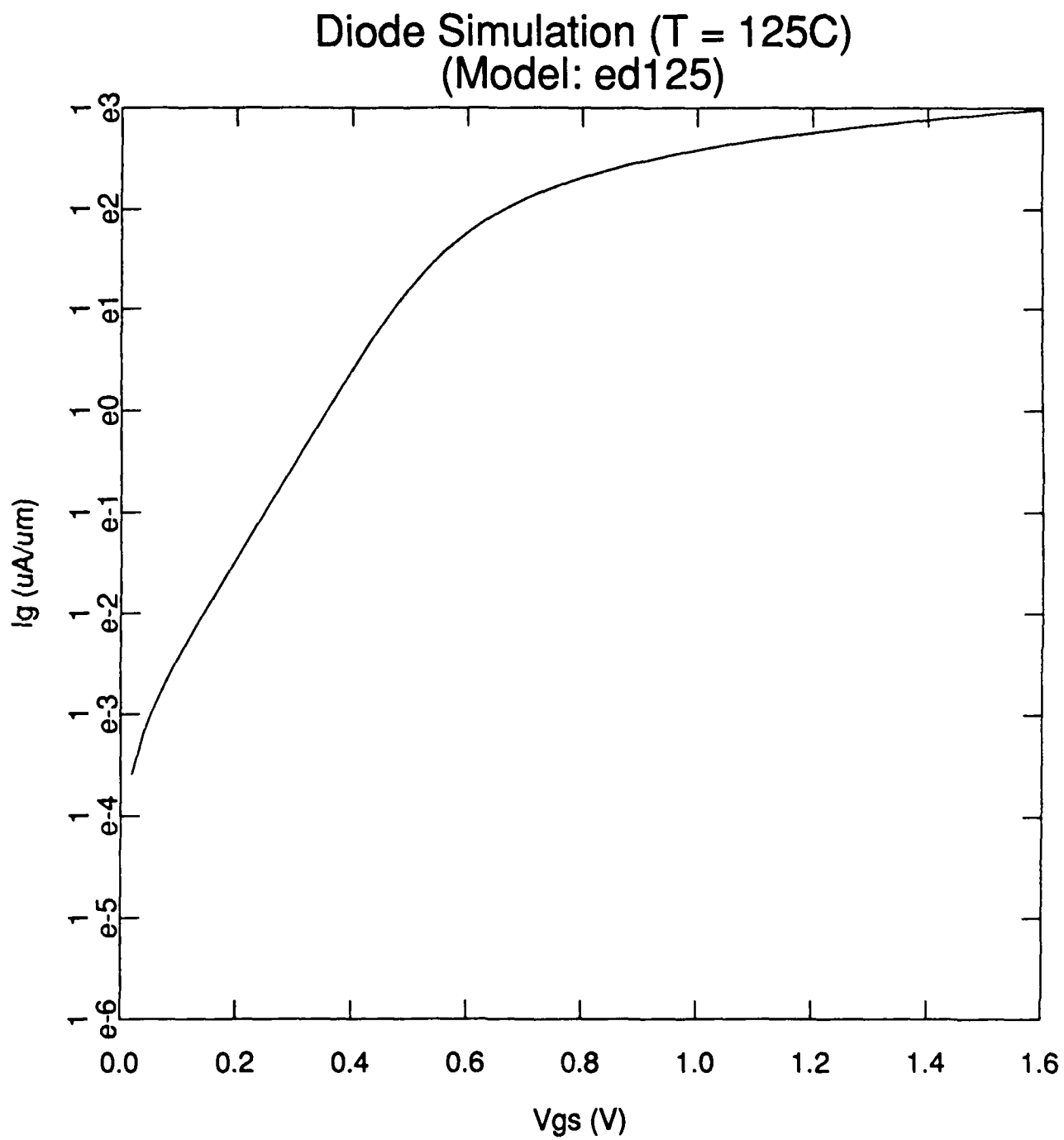


Figure 37. Ig vs. Vgs for ed125 Diode Simulation at 125C (semilog).

Diode Simulation (T = 125C)
(Model: ed125)

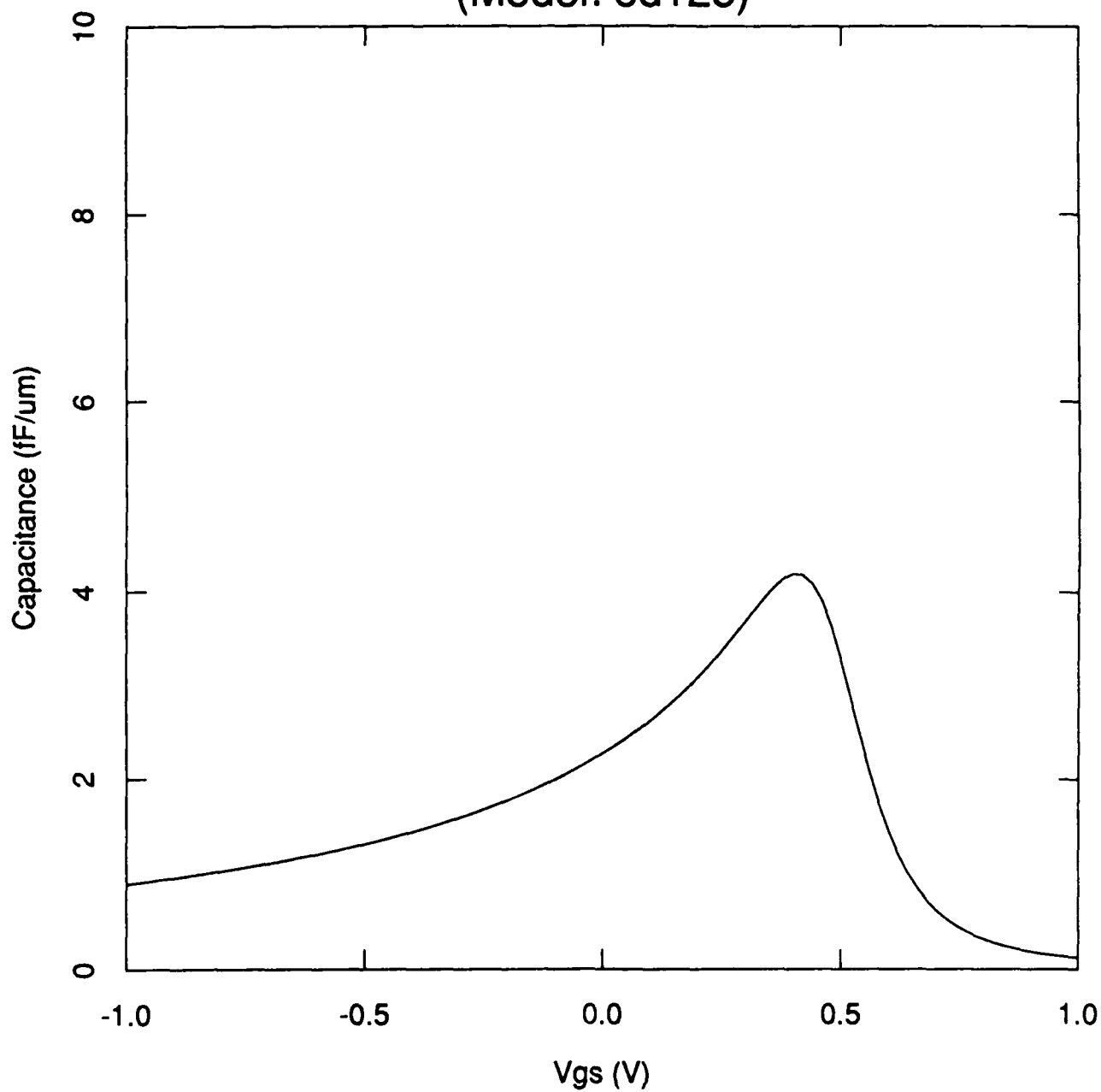


Figure 38. C vs. V_{ds} for ed125 Diode Simulation at 125C.

Table 1. Id and Ig vs. Vds (Vgs stepped) for d25 DHFET Simulation at 25C.

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
0.00	-1.00	1.376e-05	-2.752e-05
0.10	-1.00	7.810e-05	-2.772e-05
0.20	-1.00	4.098e-04	-2.792e-05
0.30	-1.00	1.160e-03	-2.812e-05
0.40	-1.00	2.450e-03	-2.832e-05
0.50	-1.00	4.384e-03	-2.852e-05
0.60	-1.00	7.053e-03	-2.872e-05
0.70	-1.00	1.054e-02	-2.892e-05
0.80	-1.00	1.493e-02	-2.912e-05
0.90	-1.00	2.029e-02	-2.932e-05
1.00	-1.00	2.667e-02	-2.952e-05
1.10	-1.00	3.416e-02	-2.972e-05
1.20	-1.00	4.279e-02	-2.992e-05
1.30	-1.00	5.263e-02	-3.012e-05
1.40	-1.00	6.372e-02	-3.033e-05
1.50	-1.00	7.611e-02	-3.053e-05
1.60	-1.00	8.984e-02	-3.073e-05
1.70	-1.00	1.049e-01	-3.093e-05
1.80	-1.00	1.215e-01	-3.113e-05
1.90	-1.00	1.394e-01	-3.133e-05
2.00	-1.00	1.589e-01	-3.153e-05
2.10	-1.00	1.798e-01	-3.173e-05
2.20	-1.00	2.023e-01	-3.193e-05
2.30	-1.00	2.264e-01	-3.213e-05
2.40	-1.00	2.520e-01	-3.233e-05
2.50	-1.00	2.792e-01	-3.253e-05
0.00	-0.80	1.335e-05	-2.671e-05
0.10	-0.80	1.816e-04	-2.691e-05
0.20	-0.80	1.049e-03	-2.712e-05
0.30	-0.80	3.007e-03	-2.731e-05
0.40	-0.80	6.360e-03	-2.752e-05
0.50	-0.80	1.137e-02	-2.772e-05
0.60	-0.80	1.824e-02	-2.792e-05
0.70	-0.80	2.719e-02	-2.812e-05
0.80	-0.80	3.837e-02	-2.832e-05
0.90	-0.80	5.194e-02	-2.852e-05
1.00	-0.80	6.801e-02	-2.872e-05
1.10	-0.80	8.671e-02	-2.892e-05
1.20	-0.80	1.081e-01	-2.912e-05
1.30	-0.80	1.323e-01	-2.932e-05
1.40	-0.80	1.594e-01	-2.952e-05
1.50	-0.80	1.894e-01	-2.972e-05
1.60	-0.80	2.224e-01	-2.992e-05
1.70	-0.80	2.584e-01	-3.012e-05
1.80	-0.80	2.973e-01	-3.032e-05
1.90	-0.80	3.394e-01	-3.052e-05
2.00	-0.80	3.844e-01	-3.072e-05
2.10	-0.80	4.325e-01	-3.092e-05
2.20	-0.80	4.836e-01	-3.112e-05
2.30	-0.80	5.377e-01	-3.133e-05

Table 1. Id and Ig vs. Vds (Vgs stepped) for d25 DHFET Simulation at 25C (page 2).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.40	-0.80	5.949e-01	-3.153e-05
2.50	-0.80	6.549e-01	-3.173e-05
0.00	-0.60	1.293e-05	-2.585e-05
0.10	-0.60	2.457e-03	-2.607e-05
0.20	-0.60	1.462e-02	-2.628e-05
0.30	-0.60	4.058e-02	-2.649e-05
0.40	-0.60	8.208e-02	-2.669e-05
0.50	-0.60	1.393e-01	-2.689e-05
0.60	-0.60	2.117e-01	-2.709e-05
0.70	-0.60	2.980e-01	-2.729e-05
0.80	-0.60	3.969e-01	-2.749e-05
0.90	-0.60	5.068e-01	-2.769e-05
1.00	-0.60	6.265e-01	-2.789e-05
1.10	-0.60	7.546e-01	-2.809e-05
1.20	-0.60	8.900e-01	-2.829e-05
1.30	-0.60	1.032e+00	-2.849e-05
1.40	-0.60	1.179e+00	-2.869e-05
1.50	-0.60	1.331e+00	-2.889e-05
1.60	-0.60	1.487e+00	-2.909e-05
1.70	-0.60	1.647e+00	-2.929e-05
1.80	-0.60	1.810e+00	-2.949e-05
1.90	-0.60	1.976e+00	-2.970e-05
2.00	-0.60	2.144e+00	-2.990e-05
2.10	-0.60	2.315e+00	-3.010e-05
2.20	-0.60	2.487e+00	-3.030e-05
2.30	-0.60	2.661e+00	-3.050e-05
2.40	-0.60	2.837e+00	-3.070e-05
2.50	-0.60	3.013e+00	-3.090e-05
0.00	-0.40	1.233e-05	-2.466e-05
0.10	-0.40	6.393e+00	-2.502e-05
0.20	-0.40	1.022e+01	-2.529e-05
0.30	-0.40	1.231e+01	-2.552e-05
0.40	-0.40	1.351e+01	-2.573e-05
0.50	-0.40	1.429e+01	-2.593e-05
0.60	-0.40	1.484e+01	-2.614e-05
0.70	-0.40	1.526e+01	-2.634e-05
0.80	-0.40	1.561e+01	-2.654e-05
0.90	-0.40	1.591e+01	-2.674e-05
1.00	-0.40	1.618e+01	-2.694e-05
1.10	-0.40	1.643e+01	-2.714e-05
1.20	-0.40	1.666e+01	-2.735e-05
1.30	-0.40	1.689e+01	-2.755e-05
1.40	-0.40	1.710e+01	-2.775e-05
1.50	-0.40	1.730e+01	-2.795e-05
1.60	-0.40	1.751e+01	-2.815e-05
1.70	-0.40	1.770e+01	-2.835e-05
1.80	-0.40	1.790e+01	-2.855e-05
1.90	-0.40	1.809e+01	-2.875e-05
2.00	-0.40	1.828e+01	-2.895e-05
2.10	-0.40	1.847e+01	-2.916e-05

Table 1. Id and Ig vs. Vds (Vgs stepped) for d25 DHFET Simulation at 25C (page 3).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.20	-0.40	1.865e+01	-2.936e-05
2.30	-0.40	1.884e+01	-2.956e-05
2.40	-0.40	1.902e+01	-2.976e-05
2.50	-0.40	1.921e+01	-2.996e-05
0.00	-0.20	1.051e-05	-2.102e-05
0.10	-0.20	1.203e+01	-2.241e-05
0.20	-0.20	2.074e+01	-2.322e-05
0.30	-0.20	2.616e+01	-2.371e-05
0.40	-0.20	2.936e+01	-2.404e-05
0.50	-0.20	3.130e+01	-2.431e-05
0.60	-0.20	3.256e+01	-2.454e-05
0.70	-0.20	3.345e+01	-2.476e-05
0.80	-0.20	3.411e+01	-2.497e-05
0.90	-0.20	3.463e+01	-2.518e-05
1.00	-0.20	3.505e+01	-2.538e-05
1.10	-0.20	3.542e+01	-2.559e-05
1.20	-0.20	3.575e+01	-2.580e-05
1.30	-0.20	3.604e+01	-2.600e-05
1.40	-0.20	3.631e+01	-2.621e-05
1.50	-0.20	3.657e+01	-2.641e-05
1.60	-0.20	3.681e+01	-2.661e-05
1.70	-0.20	3.704e+01	-2.682e-05
1.80	-0.20	3.726e+01	-2.702e-05
1.90	-0.20	3.748e+01	-2.723e-05
2.00	-0.20	3.768e+01	-2.743e-05
2.10	-0.20	3.789e+01	-2.763e-05
2.20	-0.20	3.809e+01	-2.784e-05
2.30	-0.20	3.829e+01	-2.804e-05
2.40	-0.20	3.848e+01	-2.824e-05
2.50	-0.20	3.868e+01	-2.845e-05
0.00	0.00	1.333e-19	-2.666e-19
0.10	0.00	1.592e+01	-8.935e-06
0.20	0.00	2.894e+01	-1.392e-05
0.30	0.00	3.826e+01	-1.664e-05
0.40	0.00	4.427e+01	-1.810e-05
0.50	0.00	4.800e+01	-1.892e-05
0.60	0.00	5.037e+01	-1.944e-05
0.70	0.00	5.195e+01	-1.982e-05
0.80	0.00	5.306e+01	-2.012e-05
0.90	0.00	5.389e+01	-2.040e-05
1.00	0.00	5.454e+01	-2.065e-05
1.10	0.00	5.507e+01	-2.089e-05
1.20	0.00	5.552e+01	-2.113e-05
1.30	0.00	5.591e+01	-2.136e-05
1.40	0.00	5.626e+01	-2.159e-05
1.50	0.00	5.657e+01	-2.181e-05
1.60	0.00	5.686e+01	-2.203e-05
1.70	0.00	5.713e+01	-2.225e-05
1.80	0.00	5.738e+01	-2.247e-05
1.90	0.00	5.763e+01	-2.269e-05

Table 1. Id and Ig vs. Vds (Vgs stepped) for d25 DHFET Simulation at 25C (page 4).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.00	0.00	5.786e+01	-2.291e-05
2.10	0.00	5.809e+01	-2.313e-05
2.20	0.00	5.830e+01	-2.335e-05
2.30	0.00	5.852e+01	-2.356e-05
2.40	0.00	5.873e+01	-2.378e-05
2.50	0.00	5.893e+01	-2.399e-05
0.00	0.20	-7.257e-05	1.451e-04
0.10	0.20	1.871e+01	8.161e-05
0.20	0.20	3.515e+01	4.518e-05
0.30	0.20	4.828e+01	2.473e-05
0.40	0.20	5.773e+01	1.366e-05
0.50	0.20	6.398e+01	7.833e-06
0.60	0.20	6.801e+01	4.712e-06
0.70	0.20	7.064e+01	2.925e-06
0.80	0.20	7.244e+01	1.791e-06
0.90	0.20	7.372e+01	9.913e-07
1.00	0.20	7.469e+01	3.720e-07
1.10	0.20	7.544e+01	-1.419e-07
1.20	0.20	7.606e+01	-5.899e-07
1.30	0.20	7.657e+01	-9.943e-07
1.40	0.20	7.701e+01	-1.368e-06
1.50	0.20	7.740e+01	-1.720e-06
1.60	0.20	7.775e+01	-2.057e-06
1.70	0.20	7.807e+01	-2.380e-06
1.80	0.20	7.837e+01	-2.694e-06
1.90	0.20	7.864e+01	-3.000e-06
2.00	0.20	7.891e+01	-3.300e-06
2.10	0.20	7.915e+01	-3.595e-06
2.20	0.20	7.939e+01	-3.885e-06
2.30	0.20	7.962e+01	-4.172e-06
2.40	0.20	7.985e+01	-4.456e-06
2.50	0.20	8.007e+01	-4.738e-06
0.00	0.40	-5.880e-04	1.176e-03
0.10	0.40	2.079e+01	7.196e-04
0.20	0.40	3.987e+01	4.519e-04
0.30	0.40	5.629e+01	2.965e-04
0.40	0.40	6.931e+01	2.086e-04
0.50	0.40	7.874e+01	1.604e-04
0.60	0.40	8.511e+01	1.346e-04
0.70	0.40	8.931e+01	1.206e-04
0.80	0.40	9.214e+01	1.125e-04
0.90	0.40	9.410e+01	1.074e-04
1.00	0.40	9.552e+01	1.040e-04
1.10	0.40	9.659e+01	1.015e-04
1.20	0.40	9.743e+01	9.958e-05
1.30	0.40	9.812e+01	9.801e-05
1.40	0.40	9.869e+01	9.668e-05
1.50	0.40	9.917e+01	9.552e-05
1.60	0.40	9.960e+01	9.449e-05
1.70	0.40	9.998e+01	9.355e-05

Table 1. Id and Ig vs. Vds (Vgs stepped) for d25 DHFET Simulation at 25C (page 5).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
1.80	0.40	1.003e+02	9.268e-05
1.90	0.40	1.006e+02	9.188e-05
2.00	0.40	1.009e+02	9.111e-05
2.10	0.40	1.012e+02	9.039e-05
2.20	0.40	1.015e+02	8.969e-05
2.30	0.40	1.017e+02	8.902e-05
2.40	0.40	1.020e+02	8.837e-05
2.50	0.40	1.022e+02	8.774e-05
0.00	0.60	-4.264e-03	8.527e-03
0.10	0.60	2.241e+01	5.252e-03
0.20	0.60	4.352e+01	3.304e-03
0.30	0.60	6.261e+01	2.148e-03
0.40	0.60	7.890e+01	1.472e-03
0.50	0.60	9.178e+01	1.085e-03
0.60	0.60	1.012e+02	8.703e-04
0.70	0.60	1.076e+02	7.523e-04
0.80	0.60	1.120e+02	6.862e-04
0.90	0.60	1.149e+02	6.470e-04
1.00	0.60	1.170e+02	6.222e-04
1.10	0.60	1.186e+02	6.053e-04
1.20	0.60	1.197e+02	5.930e-04
1.30	0.60	1.207e+02	5.836e-04
1.40	0.60	1.214e+02	5.760e-04
1.50	0.60	1.220e+02	5.698e-04
1.60	0.60	1.226e+02	5.646e-04
1.70	0.60	1.230e+02	5.600e-04
1.80	0.60	1.234e+02	5.559e-04
1.90	0.60	1.238e+02	5.522e-04
2.00	0.60	1.241e+02	5.489e-04
2.10	0.60	1.244e+02	5.458e-04
2.20	0.60	1.247e+02	5.429e-04
2.30	0.60	1.250e+02	5.401e-04
2.40	0.60	1.253e+02	5.375e-04
2.50	0.60	1.255e+02	5.351e-04
0.00	0.80	-3.048e-02	6.096e-02
0.10	0.80	2.370e+01	3.751e-02
0.20	0.80	4.643e+01	2.343e-02
0.30	0.80	6.763e+01	1.497e-02
0.40	0.80	8.668e+01	9.919e-03
0.50	0.80	1.029e+02	6.941e-03
0.60	0.80	1.156e+02	5.222e-03
0.70	0.80	1.250e+02	4.252e-03
0.80	0.80	1.316e+02	3.707e-03
0.90	0.80	1.361e+02	3.393e-03
1.00	0.80	1.392e+02	3.202e-03
1.10	0.80	1.414e+02	3.079e-03
1.20	0.80	1.431e+02	2.994e-03
1.30	0.80	1.443e+02	2.932e-03
1.40	0.80	1.453e+02	2.885e-03
1.50	0.80	1.461e+02	2.847e-03

Table 1. Id and Ig vs. Vds (Vgs stepped) for d25 DHFET Simulation at 25C (page 6).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
1.60	0.80	1.468e+02	2.816e-03
1.70	0.80	1.474e+02	2.790e-03
1.80	0.80	1.478e+02	2.767e-03
1.90	0.80	1.483e+02	2.747e-03
2.00	0.80	1.487e+02	2.730e-03
2.10	0.80	1.490e+02	2.714e-03
2.20	0.80	1.494e+02	2.699e-03
2.30	0.80	1.497e+02	2.685e-03
2.40	0.80	1.500e+02	2.672e-03
2.50	0.80	1.502e+02	2.660e-03
0.00	1.00	-2.169e-01	4.339e-01
0.10	1.00	2.468e+01	2.669e-01
0.20	1.00	4.877e+01	1.658e-01
0.30	1.00	7.168e+01	1.046e-01
0.40	1.00	9.297e+01	6.755e-02
0.50	1.00	1.120e+02	4.531e-02
0.60	1.00	1.282e+02	3.211e-02
0.70	1.00	1.410e+02	2.441e-02
0.80	1.00	1.505e+02	2.000e-02
0.90	1.00	1.573e+02	1.748e-02
1.00	1.00	1.619e+02	1.600e-02
1.10	1.00	1.652e+02	1.508e-02
1.20	1.00	1.676e+02	1.448e-02
1.30	1.00	1.693e+02	1.406e-02
1.40	1.00	1.706e+02	1.376e-02
1.50	1.00	1.717e+02	1.352e-02
1.60	1.00	1.725e+02	1.333e-02
1.70	1.00	1.733e+02	1.318e-02
1.80	1.00	1.739e+02	1.305e-02
1.90	1.00	1.744e+02	1.294e-02
2.00	1.00	1.748e+02	1.285e-02
2.10	1.00	1.753e+02	1.276e-02
2.20	1.00	1.756e+02	1.268e-02
2.30	1.00	1.760e+02	1.261e-02
2.40	1.00	1.763e+02	1.255e-02
2.50	1.00	1.766e+02	1.249e-02

Table 2. Id and Ig vs. Vgs (Vds stepped) for d25 DHFET Simulation at 25C.

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
0.20	-1.00	4.098e-04	-2.792e-05
0.20	-0.90	6.106e-04	-2.752e-05
0.20	-0.80	1.049e-03	-2.712e-05
0.20	-0.70	2.408e-03	-2.671e-05
0.20	-0.60	1.462e-02	-2.628e-05
0.20	-0.50	4.095e+00	-2.583e-05
0.20	-0.40	1.022e+01	-2.529e-05
0.20	-0.30	1.578e+01	-2.453e-05
0.20	-0.20	2.074e+01	-2.322e-05
0.20	-0.10	2.512e+01	-2.046e-05
0.20	0.00	2.894e+01	-1.392e-05
0.20	0.10	3.226e+01	2.542e-06
0.20	0.20	3.515e+01	4.518e-05
0.20	0.30	3.766e+01	1.570e-04
0.20	0.40	3.987e+01	4.519e-04
0.20	0.50	4.180e+01	1.233e-03
0.20	0.60	4.352e+01	3.304e-03
0.20	0.70	4.505e+01	8.804e-03
0.20	0.80	4.643e+01	2.343e-02
0.20	0.90	4.767e+01	6.232e-02
0.20	1.00	4.877e+01	1.658e-01
0.40	-1.00	2.450e-03	-2.832e-05
0.40	-0.90	3.683e-03	-2.792e-05
0.40	-0.80	6.360e-03	-2.752e-05
0.40	-0.70	1.456e-02	-2.711e-05
0.40	-0.60	8.208e-02	-2.669e-05
0.40	-0.50	5.388e+00	-2.624e-05
0.40	-0.40	1.351e+01	-2.573e-05
0.40	-0.30	2.152e+01	-2.507e-05
0.40	-0.20	2.936e+01	-2.404e-05
0.40	-0.10	3.696e+01	-2.214e-05
0.40	0.00	4.427e+01	-1.810e-05
0.40	0.10	5.121e+01	-8.786e-06
0.40	0.20	5.773e+01	1.366e-05
0.40	0.30	6.377e+01	6.916e-05
0.40	0.40	6.931e+01	2.086e-04
0.40	0.50	7.435e+01	5.629e-04
0.40	0.60	7.890e+01	1.472e-03
0.40	0.70	8.300e+01	3.819e-03
0.40	0.80	8.668e+01	9.919e-03
0.40	0.90	8.999e+01	2.584e-02
0.40	1.00	9.297e+01	6.755e-02
0.60	-1.00	7.053e-03	-2.872e-05
0.60	-0.90	1.060e-02	-2.832e-05
0.60	-0.80	1.824e-02	-2.792e-05
0.60	-0.70	4.129e-02	-2.751e-05
0.60	-0.60	2.117e-01	-2.709e-05
0.60	-0.50	6.051e+00	-2.664e-05
0.60	-0.40	1.484e+01	-2.614e-05
0.60	-0.30	2.368e+01	-2.550e-05

Table 2. Id and Ig vs. Vgs (Vds stepped) for d25 DHFET Simulation at 25C (page 2).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
0.60	-0.20	3.256e+01	-2.454e-05
0.60	-0.10	4.147e+01	-2.284e-05
0.60	0.00	5.037e+01	-1.944e-05
0.60	0.10	5.923e+01	-1.204e-05
0.60	0.20	6.801e+01	4.712e-06
0.60	0.30	7.665e+01	4.351e-05
0.60	0.40	8.511e+01	1.346e-04
0.60	0.50	9.330e+01	3.510e-04
0.60	0.60	1.012e+02	8.703e-04
0.60	0.70	1.086e+02	2.130e-03
0.60	0.80	1.156e+02	5.222e-03
0.60	0.90	1.222e+02	1.289e-02
0.60	1.00	1.282e+02	3.211e-02
0.80	-1.00	1.493e-02	-2.912e-05
0.80	-0.90	2.239e-02	-2.872e-05
0.80	-0.80	3.837e-02	-2.832e-05
0.80	-0.70	8.561e-02	-2.791e-05
0.80	-0.60	3.969e-01	-2.749e-05
0.80	-0.50	6.540e+00	-2.704e-05
0.80	-0.40	1.561e+01	-2.654e-05
0.80	-0.30	2.480e+01	-2.591e-05
0.80	-0.20	3.411e+01	-2.497e-05
0.80	-0.10	4.353e+01	-2.334e-05
0.80	0.00	5.306e+01	-2.012e-05
0.80	0.10	6.270e+01	-1.329e-05
0.80	0.20	7.244e+01	1.791e-06
0.80	0.30	8.225e+01	3.568e-05
0.80	0.40	9.214e+01	1.125e-04
0.80	0.50	1.020e+02	2.872e-04
0.80	0.60	1.120e+02	6.862e-04
0.80	0.70	1.218e+02	1.601e-03
0.80	0.80	1.316e+02	3.707e-03
0.80	0.90	1.412e+02	8.589e-03
0.80	1.00	1.505e+02	2.000e-02
1.00	-1.00	2.667e-02	-2.952e-05
1.00	-0.90	3.990e-02	-2.912e-05
1.00	-0.80	6.801e-02	-2.872e-05
1.00	-0.70	1.493e-01	-2.831e-05
1.00	-0.60	6.265e-01	-2.789e-05
1.00	-0.50	6.965e+00	-2.744e-05
1.00	-0.40	1.618e+01	-2.694e-05
1.00	-0.30	2.554e+01	-2.631e-05
1.00	-0.20	3.505e+01	-2.538e-05
1.00	-0.10	4.472e+01	-2.378e-05
1.00	0.00	5.454e+01	-2.065e-05
1.00	0.10	6.453e+01	-1.405e-05
1.00	0.20	7.469e+01	3.720e-07
1.00	0.30	8.502e+01	3.241e-05
1.00	0.40	9.552e+01	1.040e-04
1.00	0.50	1.062e+02	2.642e-04

Table 2. Id and Ig vs. Vgs (Vds stepped) for d25 DHFET Simulation at 25C (page 3).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
1.00	0.60	1.170e+02	6.222e-04
1.00	0.70	1.281e+02	1.421e-03
1.00	0.80	1.392e+02	3.202e-03
1.00	0.90	1.505e+02	7.169e-03
1.00	1.00	1.619e+02	1.600e-02
1.20	-1.00	4.279e-02	-2.992e-05
1.20	-0.90	6.383e-02	-2.952e-05
1.20	-0.80	1.081e-01	-2.912e-05
1.20	-0.70	2.331e-01	-2.871e-05
1.20	-0.60	8.900e-01	-2.829e-05
1.20	-0.50	7.361e+00	-2.785e-05
1.20	-0.40	1.666e+01	-2.735e-05
1.20	-0.30	2.612e+01	-2.672e-05
1.20	-0.20	3.575e+01	-2.580e-05
1.20	-0.10	4.554e+01	-2.421e-05
1.20	0.00	5.552e+01	-2.113e-05
1.20	0.10	6.569e+01	-1.466e-05
1.20	0.20	7.606e+01	-5.899e-07
1.20	0.30	8.663e+01	3.051e-05
1.20	0.40	9.743e+01	9.958e-05
1.20	0.50	1.085e+02	2.530e-04
1.20	0.60	1.197e+02	5.930e-04
1.20	0.70	1.313e+02	1.344e-03
1.20	0.80	1.431e+02	2.994e-03
1.20	0.90	1.552e+02	6.608e-03
1.20	1.00	1.676e+02	1.448e-02
1.40	-1.00	6.372e-02	-3.033e-05
1.40	-0.90	9.474e-02	-2.992e-05
1.40	-0.80	1.594e-01	-2.952e-05
1.40	-0.70	3.373e-01	-2.911e-05
1.40	-0.60	1.179e+00	-2.869e-05
1.40	-0.50	7.741e+00	-2.825e-05
1.40	-0.40	1.710e+01	-2.775e-05
1.40	-0.30	2.662e+01	-2.712e-05
1.40	-0.20	3.631e+01	-2.621e-05
1.40	-0.10	4.619e+01	-2.464e-05
1.40	0.00	5.626e+01	-2.159e-05
1.40	0.10	6.653e+01	-1.521e-05
1.40	0.20	7.701e+01	-1.368e-06
1.40	0.30	8.773e+01	2.913e-05
1.40	0.40	9.869e+01	9.668e-05
1.40	0.50	1.099e+02	2.462e-04
1.40	0.60	1.214e+02	5.760e-04
1.40	0.70	1.332e+02	1.301e-03
1.40	0.80	1.453e+02	2.885e-03
1.40	0.90	1.578e+02	6.327e-03
1.40	1.00	1.706e+02	1.376e-02
1.60	-1.00	8.984e-02	-3.073e-05
1.60	-0.90	1.331e-01	-3.032e-05
1.60	-0.80	2.224e-01	-2.992e-05

Table 2. Id and Ig vs. Vgs (Vds stepped) for d25 DHFET Simulation at 25C (page 4).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
1.60	-0.70	4.615e-01	-2.951e-05
1.60	-0.60	1.487e+00	-2.909e-05
1.60	-0.50	8.112e+00	-2.865e-05
1.60	-0.40	1.751e+01	-2.815e-05
1.60	-0.30	2.707e+01	-2.753e-05
1.60	-0.20	3.681e+01	-2.661e-05
1.60	-0.10	4.673e+01	-2.505e-05
1.60	0.00	5.686e+01	-2.203e-05
1.60	0.10	6.719e+01	-1.572e-05
1.60	0.20	7.775e+01	-2.057e-06
1.60	0.30	8.855e+01	2.802e-05
1.60	0.40	9.960e+01	9.449e-05
1.60	0.50	1.109e+02	2.413e-04
1.60	0.60	1.226e+02	5.646e-04
1.60	0.70	1.345e+02	1.273e-03
1.60	0.80	1.468e+02	2.816e-03
1.60	0.90	1.595e+02	6.157e-03
1.60	1.00	1.725e+02	1.333e-02
1.80	-1.00	1.215e-01	-3.113e-05
1.80	-0.90	1.793e-01	-3.073e-05
1.80	-0.80	2.973e-01	-3.032e-05
1.80	-0.70	6.049e-01	-2.991e-05
1.80	-0.60	1.810e+00	-2.949e-05
1.80	-0.50	8.478e+00	-2.905e-05
1.80	-0.40	1.790e+01	-2.855e-05
1.80	-0.30	2.749e+01	-2.793e-05
1.80	-0.20	3.726e+01	-2.702e-05
1.80	-0.10	4.722e+01	-2.547e-05
1.80	0.00	5.738e+01	-2.247e-05
1.80	0.10	6.776e+01	-1.622e-05
1.80	0.20	7.837e+01	-2.694e-06
1.80	0.30	8.922e+01	2.704e-05
1.80	0.40	1.003e+02	9.268e-05
1.80	0.50	1.117e+02	2.375e-04
1.80	0.60	1.234e+02	5.559e-04
1.80	0.70	1.355e+02	1.252e-03
1.80	0.80	1.478e+02	2.767e-03
1.80	0.90	1.606e+02	6.040e-03
1.80	1.00	1.739e+02	1.305e-02
2.00	-1.00	1.589e-01	-3.153e-05
2.00	-0.90	2.337e-01	-3.113e-05
2.00	-0.80	3.844e-01	-3.072e-05
2.00	-0.70	7.666e-01	-3.032e-05
2.00	-0.60	2.144e+00	-2.990e-05
2.00	-0.50	8.840e+00	-2.945e-05
2.00	-0.40	1.828e+01	-2.895e-05
2.00	-0.30	2.789e+01	-2.833e-05
2.00	-0.20	3.768e+01	-2.743e-05
2.00	-0.10	4.767e+01	-2.589e-05
2.00	0.00	5.786e+01	-2.291e-05

Table 2. Id and Ig vs. Vgs (Vds stepped) for d25 DHFET Simulation at 25C (page 5).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.00	0.10	6.827e+01	-1.671e-05
2.00	0.20	7.891e+01	-3.300e-06
2.00	0.30	8.979e+01	2.615e-05
2.00	0.40	1.009e+02	9.111e-05
2.00	0.50	1.124e+02	2.343e-04
2.00	0.60	1.241e+02	5.489e-04
2.00	0.70	1.362e+02	1.236e-03
2.00	0.80	1.487e+02	2.730e-03
2.00	0.90	1.615e+02	5.951e-03
2.00	1.00	1.748e+02	1.285e-02
2.20	-1.00	2.023e-01	-3.193e-05
2.20	-0.90	2.963e-01	-3.153e-05
2.20	-0.80	4.836e-01	-3.112e-05
2.20	-0.70	9.455e-01	-3.072e-05
2.20	-0.60	2.487e+00	-3.030e-05
2.20	-0.50	9.200e+00	-2.985e-05
2.20	-0.40	1.865e+01	-2.936e-05
2.20	-0.30	2.828e+01	-2.874e-05
2.20	-0.20	3.809e+01	-2.784e-05
2.20	-0.10	4.809e+01	-2.630e-05
2.20	0.00	5.830e+01	-2.335e-05
2.20	0.10	6.873e+01	-1.719e-05
2.20	0.20	7.939e+01	-3.885e-06
2.20	0.30	9.031e+01	2.531e-05
2.20	0.40	1.015e+02	8.969e-05
2.20	0.50	1.130e+02	2.315e-04
2.20	0.60	1.247e+02	5.429e-04
2.20	0.70	1.369e+02	1.223e-03
2.20	0.80	1.494e+02	2.699e-03
2.20	0.90	1.623e+02	5.880e-03
2.20	1.00	1.756e+02	1.268e-02
2.40	-1.00	2.520e-01	-3.233e-05
2.40	-0.90	3.675e-01	-3.193e-05
2.40	-0.80	5.949e-01	-3.153e-05
2.40	-0.70	1.140e+00	-3.112e-05
2.40	-0.60	2.837e+00	-3.070e-05
2.40	-0.50	9.558e+00	-3.025e-05
2.40	-0.40	1.902e+01	-2.976e-05
2.40	-0.30	2.866e+01	-2.914e-05
2.40	-0.20	3.848e+01	-2.824e-05
2.40	-0.10	4.850e+01	-2.672e-05
2.40	0.00	5.873e+01	-2.378e-05
2.40	0.10	6.917e+01	-1.766e-05
2.40	0.20	7.985e+01	-4.456e-06
2.40	0.30	9.078e+01	2.452e-05
2.40	0.40	1.020e+02	8.837e-05
2.40	0.50	1.135e+02	2.290e-04
2.40	0.60	1.253e+02	5.375e-04
2.40	0.70	1.374e+02	1.211e-03
2.40	0.80	1.500e+02	2.672e-03

Table 2. Id and Ig vs. Vgs (Vds stepped) for d25 DHFET Simulation at 25C (page 6).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.40	0.90	1.629e+02	5.821e-03
2.40	1.00	1.763e+02	1.255e-02

Table 3. I_g vs. V_{gs} ($V_{ds} = 0$) for d25 DHFET Simulation at 25C.

V_{gs} (V)	I_g ($\mu A/\mu m$)
0.00	-2.666e-19
0.02	5.188e-06
0.04	1.148e-05
0.06	1.913e-05
0.08	2.842e-05
0.10	3.971e-05
0.12	5.344e-05
0.14	7.012e-05
0.16	9.042e-05
0.18	1.151e-04
0.20	1.451e-04
0.22	1.817e-04
0.24	2.261e-04
0.26	2.802e-04
0.28	3.460e-04
0.30	4.261e-04
0.32	5.236e-04
0.34	6.421e-04
0.36	7.865e-04
0.38	9.622e-04
0.40	1.176e-03
0.42	1.436e-03
0.44	1.753e-03
0.46	2.138e-03
0.48	2.607e-03
0.50	3.178e-03
0.52	3.873e-03
0.54	4.719e-03
0.56	5.749e-03
0.58	7.002e-03
0.60	8.527e-03
0.62	1.038e-02
0.64	1.264e-02
0.66	1.539e-02
0.68	1.874e-02
0.70	2.281e-02
0.72	2.777e-02
0.74	3.380e-02
0.76	4.115e-02
0.78	5.008e-02
0.80	6.096e-02
0.82	7.420e-02
0.84	9.030e-02
0.86	1.099e-01
0.88	1.337e-01
0.90	1.627e-01
0.92	1.980e-01
0.94	2.410e-01
0.96	2.932e-01
0.98	3.567e-01

Table 3. I_g vs. V_{ds} ($V_{ds} = 0$) for d25 DHFET Simulation at 25C (page 2).

V_{gs} (V)	I_g ($\mu A/\mu m$)
1.00	4.339e-01
1.02	5.277e-01
1.04	6.417e-01
1.06	7.802e-01
1.08	9.483e-01
1.10	1.152e+00
1.12	1.400e+00
1.14	1.700e+00
1.16	2.063e+00
1.18	2.502e+00
1.20	3.032e+00
1.22	3.671e+00
1.24	4.441e+00
1.26	5.365e+00
1.28	6.472e+00
1.30	7.794e+00
1.32	9.367e+00
1.34	1.123e+01
1.36	1.343e+01
1.38	1.601e+01
1.40	1.901e+01
1.42	2.250e+01
1.44	2.651e+01
1.46	3.110e+01
1.48	3.629e+01
1.50	4.214e+01
1.52	4.865e+01
1.54	5.586e+01
1.56	6.378e+01
1.58	7.240e+01
1.60	8.172e+01

Table 4. Cgd and Cgs vs. Vds (Vgs stepped) for d25 DHFET Simulation at 25C.

Vds (V)	Vgs (V)	Cgd (fF/ μ m)	Cgs (fF/ μ m)
0.00	-1.00	2.604e-01	7.802e-01
0.50	-1.00	2.604e-01	7.802e-01
1.00	-1.00	2.604e-01	7.802e-01
1.50	-1.00	2.604e-01	7.802e-01
2.00	-1.00	2.604e-01	7.802e-01
2.50	-1.00	2.604e-01	7.802e-01
0.00	-0.75	2.604e-01	9.139e-01
0.50	-0.75	2.604e-01	9.139e-01
1.00	-0.75	2.604e-01	9.139e-01
1.50	-0.75	2.604e-01	9.139e-01
2.00	-0.75	2.604e-01	9.139e-01
2.50	-0.75	2.604e-01	9.139e-01
0.00	-0.50	2.604e-01	1.073e+00
0.50	-0.50	2.604e-01	1.073e+00
1.00	-0.50	2.604e-01	1.073e+00
1.50	-0.50	2.604e-01	1.073e+00
2.00	-0.50	2.604e-01	1.073e+00
2.50	-0.50	2.604e-01	1.073e+00
0.00	-0.25	2.604e-01	1.262e+00
0.50	-0.25	2.604e-01	1.262e+00
1.00	-0.25	2.604e-01	1.262e+00
1.50	-0.25	2.604e-01	1.262e+00
2.00	-0.25	2.604e-01	1.262e+00
2.50	-0.25	2.604e-01	1.262e+00
0.00	0.00	2.604e-01	1.487e+00
0.50	0.00	2.604e-01	1.487e+00
1.00	0.00	2.604e-01	1.487e+00
1.50	0.00	2.604e-01	1.487e+00
2.00	0.00	2.604e-01	1.487e+00
2.50	0.00	2.604e-01	1.487e+00
0.00	0.25	2.604e-01	1.756e+00
0.50	0.25	2.604e-01	1.756e+00
1.00	0.25	2.604e-01	1.756e+00
1.50	0.25	2.604e-01	1.756e+00
2.00	0.25	2.604e-01	1.756e+00
2.50	0.25	2.604e-01	1.756e+00
0.00	0.50	2.604e-01	2.078e+00
0.50	0.50	2.604e-01	2.078e+00
1.00	0.50	2.604e-01	2.078e+00
1.50	0.50	2.604e-01	2.078e+00
2.00	0.50	2.604e-01	2.078e+00
2.50	0.50	2.604e-01	2.078e+00
0.00	0.75	2.604e-01	2.465e+00
0.50	0.75	2.604e-01	2.465e+00
1.00	0.75	2.604e-01	2.465e+00
1.50	0.75	2.604e-01	2.465e+00
2.00	0.75	2.604e-01	2.465e+00
2.50	0.75	2.604e-01	2.465e+00

Table 5. Cgd and Cgs vs. Vgs (Vds stepped) for d25 DHFET Simulation at 25C.

Vds (V)	Vgs (V)	Cgd (fF/ μ m)	Cgs (fF/ μ m)
0.00	-1.00	2.604e-01	7.802e-01
0.00	-0.90	2.604e-01	8.310e-01
0.00	-0.80	2.604e-01	8.853e-01
0.00	-0.70	2.604e-01	9.435e-01
0.00	-0.60	2.604e-01	1.006e+00
0.00	-0.50	2.604e-01	1.073e+00
0.00	-0.40	2.604e-01	1.144e+00
0.00	-0.30	2.604e-01	1.221e+00
0.00	-0.20	2.604e-01	1.303e+00
0.00	-0.10	2.604e-01	1.392e+00
0.00	0.00	2.604e-01	1.487e+00
0.00	0.10	2.604e-01	1.589e+00
0.00	0.20	2.604e-01	1.698e+00
0.00	0.30	2.604e-01	1.816e+00
0.00	0.40	2.604e-01	1.942e+00
0.00	0.50	2.604e-01	2.078e+00
0.00	0.60	2.604e-01	2.224e+00
0.00	0.70	2.604e-01	2.382e+00
0.00	0.80	2.604e-01	2.552e+00
0.00	0.90	2.604e-01	2.734e+00
0.00	1.00	2.604e-01	2.931e+00
2.50	-1.00	2.604e-01	7.802e-01
2.50	-0.90	2.604e-01	8.310e-01
2.50	-0.80	2.604e-01	8.853e-01
2.50	-0.70	2.604e-01	9.435e-01
2.50	-0.60	2.604e-01	1.006e+00
2.50	-0.50	2.604e-01	1.073e+00
2.50	-0.40	2.604e-01	1.144e+00
2.50	-0.30	2.604e-01	1.221e+00
2.50	-0.20	2.604e-01	1.303e+00
2.50	-0.10	2.604e-01	1.392e+00
2.50	0.00	2.604e-01	1.487e+00
2.50	0.10	2.604e-01	1.589e+00
2.50	0.20	2.604e-01	1.698e+00
2.50	0.30	2.604e-01	1.816e+00
2.50	0.40	2.604e-01	1.942e+00
2.50	0.50	2.604e-01	2.078e+00
2.50	0.60	2.604e-01	2.224e+00
2.50	0.70	2.604e-01	2.382e+00
2.50	0.80	2.604e-01	2.552e+00
2.50	0.90	2.604e-01	2.734e+00
2.50	1.00	2.604e-01	2.931e+00

Table 6. Id and Ig vs. Vds (Vgs stepped) for d125 DHFET Simulation at 125C.

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
0.00	-1.00	1.023e-03	-2.045e-03
0.10	-1.00	1.062e-03	-2.046e-03
0.20	-1.00	1.335e-03	-2.046e-03
0.30	-1.00	2.066e-03	-2.046e-03
0.40	-1.00	3.478e-03	-2.046e-03
0.50	-1.00	5.789e-03	-2.047e-03
0.60	-1.00	9.212e-03	-2.047e-03
0.70	-1.00	1.395e-02	-2.047e-03
0.80	-1.00	2.022e-02	-2.047e-03
0.90	-1.00	2.820e-02	-2.048e-03
1.00	-1.00	3.809e-02	-2.048e-03
1.10	-1.00	5.007e-02	-2.048e-03
1.20	-1.00	6.432e-02	-2.048e-03
1.30	-1.00	8.099e-02	-2.049e-03
1.40	-1.00	1.002e-01	-2.049e-03
1.50	-1.00	1.222e-01	-2.049e-03
1.60	-1.00	1.471e-01	-2.049e-03
1.70	-1.00	1.749e-01	-2.049e-03
1.80	-1.00	2.059e-01	-2.050e-03
1.90	-1.00	2.401e-01	-2.050e-03
2.00	-1.00	2.776e-01	-2.050e-03
2.10	-1.00	3.185e-01	-2.050e-03
2.20	-1.00	3.629e-01	-2.051e-03
2.30	-1.00	4.108e-01	-2.051e-03
2.40	-1.00	4.624e-01	-2.051e-03
2.50	-1.00	5.176e-01	-2.051e-03
0.00	-0.80	1.021e-03	-2.042e-03
0.10	-0.80	1.155e-03	-2.043e-03
0.20	-0.80	2.069e-03	-2.043e-03
0.30	-0.80	4.514e-03	-2.044e-03
0.40	-0.80	9.215e-03	-2.044e-03
0.50	-0.80	1.686e-02	-2.044e-03
0.60	-0.80	2.810e-02	-2.045e-03
0.70	-0.80	4.352e-02	-2.045e-03
0.80	-0.80	6.369e-02	-2.045e-03
0.90	-0.80	8.908e-02	-2.045e-03
1.00	-0.80	1.201e-01	-2.046e-03
1.10	-0.80	1.572e-01	-2.046e-03
1.20	-0.80	2.006e-01	-2.046e-03
1.30	-0.80	2.505e-01	-2.046e-03
1.40	-0.80	3.073e-01	-2.046e-03
1.50	-0.80	3.709e-01	-2.047e-03
1.60	-0.80	4.415e-01	-2.047e-03
1.70	-0.80	5.190e-01	-2.047e-03
1.80	-0.80	6.036e-01	-2.047e-03
1.90	-0.80	6.951e-01	-2.048e-03
2.00	-0.80	7.934e-01	-2.048e-03
2.10	-0.80	8.984e-01	-2.048e-03
2.20	-0.80	1.010e+00	-2.048e-03
2.30	-0.80	1.128e+00	-2.049e-03

Table 6. Id and Ig vs. Vds (Vgs stepped) for d125 DHFET Simulation at 125C (page 2).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.40	-0.80	1.252e+00	-2.049e-03
2.50	-0.80	1.383e+00	-2.049e-03
0.00	-0.60	1.013e-03	-2.027e-03
0.10	-0.60	6.181e-03	-2.032e-03
0.20	-0.60	3.872e-02	-2.034e-03
0.30	-0.60	1.134e-01	-2.035e-03
0.40	-0.60	2.313e-01	-2.036e-03
0.50	-0.60	3.858e-01	-2.036e-03
0.60	-0.60	5.685e-01	-2.037e-03
0.70	-0.60	7.721e-01	-2.037e-03
0.80	-0.60	9.909e-01	-2.037e-03
0.90	-0.60	1.221e+00	-2.038e-03
1.00	-0.60	1.459e+00	-2.038e-03
1.10	-0.60	1.703e+00	-2.038e-03
1.20	-0.60	1.952e+00	-2.038e-03
1.30	-0.60	2.204e+00	-2.039e-03
1.40	-0.60	2.459e+00	-2.039e-03
1.50	-0.60	2.716e+00	-2.039e-03
1.60	-0.60	2.975e+00	-2.039e-03
1.70	-0.60	3.235e+00	-2.040e-03
1.80	-0.60	3.496e+00	-2.040e-03
1.90	-0.60	3.759e+00	-2.040e-03
2.00	-0.60	4.022e+00	-2.041e-03
2.10	-0.60	4.285e+00	-2.041e-03
2.20	-0.60	4.550e+00	-2.041e-03
2.30	-0.60	4.814e+00	-2.041e-03
2.40	-0.60	5.080e+00	-2.042e-03
2.50	-0.60	5.345e+00	-2.042e-03
0.00	-0.40	9.791e-04	-1.958e-03
0.10	-0.40	5.839e+00	-1.983e-03
0.20	-0.40	9.942e+00	-1.997e-03
0.30	-0.40	1.240e+01	-2.003e-03
0.40	-0.40	1.384e+01	-2.007e-03
0.50	-0.40	1.476e+01	-2.008e-03
0.60	-0.40	1.540e+01	-2.010e-03
0.70	-0.40	1.589e+01	-2.010e-03
0.80	-0.40	1.631e+01	-2.011e-03
0.90	-0.40	1.667e+01	-2.011e-03
1.00	-0.40	1.699e+01	-2.012e-03
1.10	-0.40	1.730e+01	-2.012e-03
1.20	-0.40	1.759e+01	-2.012e-03
1.30	-0.40	1.787e+01	-2.013e-03
1.40	-0.40	1.815e+01	-2.013e-03
1.50	-0.40	1.841e+01	-2.013e-03
1.60	-0.40	1.868e+01	-2.014e-03
1.70	-0.40	1.894e+01	-2.014e-03
1.80	-0.40	1.920e+01	-2.014e-03
1.90	-0.40	1.945e+01	-2.015e-03
2.00	-0.40	1.971e+01	-2.015e-03
2.10	-0.40	1.996e+01	-2.015e-03

Table 6. Id and Ig vs. Vds (Vgs stepped) for d125 DHFET Simulation at 125C (page 3).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.20	-0.40	2.021e+01	-2.016e-03
2.30	-0.40	2.046e+01	-2.016e-03
2.40	-0.40	2.071e+01	-2.016e-03
2.50	-0.40	2.096e+01	-2.017e-03
0.00	-0.20	8.126e-04	-1.625e-03
0.10	-0.20	1.058e+01	-1.753e-03
0.20	-0.20	1.901e+01	-1.826e-03
0.30	-0.20	2.475e+01	-1.866e-03
0.40	-0.20	2.827e+01	-1.888e-03
0.50	-0.20	3.040e+01	-1.899e-03
0.60	-0.20	3.175e+01	-1.905e-03
0.70	-0.20	3.268e+01	-1.908e-03
0.80	-0.20	3.337e+01	-1.910e-03
0.90	-0.20	3.392e+01	-1.912e-03
1.00	-0.20	3.438e+01	-1.913e-03
1.10	-0.20	3.478e+01	-1.914e-03
1.20	-0.20	3.514e+01	-1.915e-03
1.30	-0.20	3.548e+01	-1.915e-03
1.40	-0.20	3.579e+01	-1.916e-03
1.50	-0.20	3.609e+01	-1.917e-03
1.60	-0.20	3.638e+01	-1.918e-03
1.70	-0.20	3.666e+01	-1.918e-03
1.80	-0.20	3.694e+01	-1.919e-03
1.90	-0.20	3.721e+01	-1.920e-03
2.00	-0.20	3.747e+01	-1.920e-03
2.10	-0.20	3.773e+01	-1.921e-03
2.20	-0.20	3.799e+01	-1.922e-03
2.30	-0.20	3.825e+01	-1.922e-03
2.40	-0.20	3.851e+01	-1.923e-03
2.50	-0.20	3.876e+01	-1.924e-03
0.00	0.00	6.085e-11	-1.217e-10
0.10	0.00	1.406e+01	-6.388e-04
0.20	0.00	2.619e+01	-1.026e-03
0.30	0.00	3.548e+01	-1.255e-03
0.40	0.00	4.177e+01	-1.384e-03
0.50	0.00	4.573e+01	-1.453e-03
0.60	0.00	4.820e+01	-1.490e-03
0.70	0.00	4.980e+01	-1.511e-03
0.80	0.00	5.091e+01	-1.523e-03
0.90	0.00	5.173e+01	-1.530e-03
1.00	0.00	5.238e+01	-1.536e-03
1.10	0.00	5.291e+01	-1.540e-03
1.20	0.00	5.336e+01	-1.544e-03
1.30	0.00	5.377e+01	-1.547e-03
1.40	0.00	5.414e+01	-1.549e-03
1.50	0.00	5.448e+01	-1.552e-03
1.60	0.00	5.480e+01	-1.554e-03
1.70	0.00	5.510e+01	-1.556e-03
1.80	0.00	5.540e+01	-1.558e-03
1.90	0.00	5.569e+01	-1.561e-03

Table 6. Id and Ig vs. Vds (Vgs stepped) for d125 DHFET Simulation at 125C (page 4).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.00	0.00	5.597e+01	-1.563e-03
2.10	0.00	5.624e+01	-1.565e-03
2.20	0.00	5.651e+01	-1.567e-03
2.30	0.00	5.677e+01	-1.569e-03
2.40	0.00	5.704e+01	-1.570e-03
2.50	0.00	5.730e+01	-1.572e-03
0.00	0.20	-3.971e-03	7.942e-03
0.10	0.20	1.669e+01	4.774e-03
0.20	0.20	3.181e+01	2.784e-03
0.30	0.20	4.444e+01	1.552e-03
0.40	0.20	5.392e+01	8.165e-04
0.50	0.20	6.037e+01	3.983e-04
0.60	0.20	6.450e+01	1.681e-04
0.70	0.20	6.714e+01	4.110e-05
0.80	0.20	6.889e+01	-3.166e-05
0.90	0.20	7.012e+01	-7.611e-05
1.00	0.20	7.104e+01	-1.055e-04
1.10	0.20	7.175e+01	-1.265e-04
1.20	0.20	7.233e+01	-1.427e-04
1.30	0.20	7.283e+01	-1.560e-04
1.40	0.20	7.327e+01	-1.675e-04
1.50	0.20	7.366e+01	-1.776e-04
1.60	0.20	7.403e+01	-1.869e-04
1.70	0.20	7.436e+01	-1.955e-04
1.80	0.20	7.468e+01	-2.036e-04
1.90	0.20	7.499e+01	-2.114e-04
2.00	0.20	7.529e+01	-2.189e-04
2.10	0.20	7.557e+01	-2.261e-04
2.20	0.20	7.585e+01	-2.331e-04
2.30	0.20	7.613e+01	-2.400e-04
2.40	0.20	7.640e+01	-2.467e-04
2.50	0.20	7.666e+01	-2.533e-04
0.00	0.40	-2.338e-02	4.676e-02
0.10	0.40	1.874e+01	3.113e-02
0.20	0.40	3.626e+01	2.110e-02
0.30	0.40	5.175e+01	1.469e-02
0.40	0.40	6.444e+01	1.069e-02
0.50	0.40	7.388e+01	8.296e-03
0.60	0.40	8.031e+01	6.918e-03
0.70	0.40	8.450e+01	6.145e-03
0.80	0.40	8.724e+01	5.707e-03
0.90	0.40	8.909e+01	5.448e-03
1.00	0.40	9.040e+01	5.284e-03
1.10	0.40	9.138e+01	5.174e-03
1.20	0.40	9.214e+01	5.093e-03
1.30	0.40	9.277e+01	5.030e-03
1.40	0.40	9.330e+01	4.978e-03
1.50	0.40	9.376e+01	4.934e-03
1.60	0.40	9.418e+01	4.895e-03
1.70	0.40	9.456e+01	4.860e-03

Table 6. Id and Ig vs. Vds (Vgs stepped) for d125 DHFET Simulation at 125C (page 5).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
1.80	0.40	9.491e+01	4.827e-03
1.90	0.40	9.524e+01	4.796e-03
2.00	0.40	9.556e+01	4.767e-03
2.10	0.40	9.586e+01	4.739e-03
2.20	0.40	9.616e+01	4.713e-03
2.30	0.40	9.644e+01	4.687e-03
2.40	0.40	9.672e+01	4.661e-03
2.50	0.40	9.699e+01	4.637e-03
0.00	0.60	-1.181e-01	2.363e-01
0.10	0.60	2.035e+01	1.595e-01
0.20	0.60	3.982e+01	1.095e-01
0.30	0.60	5.770e+01	7.698e-02
0.40	0.60	7.327e+01	5.606e-02
0.50	0.60	8.586e+01	4.295e-02
0.60	0.60	9.518e+01	3.506e-02
0.70	0.60	1.016e+02	3.048e-02
0.80	0.60	1.058e+02	2.786e-02
0.90	0.60	1.086e+02	2.634e-02
1.00	0.60	1.105e+02	2.542e-02
1.10	0.60	1.119e+02	2.482e-02
1.20	0.60	1.129e+02	2.441e-02
1.30	0.60	1.137e+02	2.411e-02
1.40	0.60	1.144e+02	2.387e-02
1.50	0.60	1.149e+02	2.367e-02
1.60	0.60	1.154e+02	2.350e-02
1.70	0.60	1.158e+02	2.335e-02
1.80	0.60	1.162e+02	2.322e-02
1.90	0.60	1.166e+02	2.310e-02
2.00	0.60	1.169e+02	2.298e-02
2.10	0.60	1.173e+02	2.288e-02
2.20	0.60	1.176e+02	2.277e-02
2.30	0.60	1.179e+02	2.267e-02
2.40	0.60	1.182e+02	2.258e-02
2.50	0.60	1.184e+02	2.249e-02
0.00	0.80	-5.780e-01	1.156e+00
0.10	0.80	2.144e+01	7.829e-01
0.20	0.80	4.260e+01	5.367e-01
0.30	0.80	6.248e+01	3.743e-01
0.40	0.80	8.055e+01	2.678e-01
0.50	0.80	9.613e+01	1.990e-01
0.60	0.80	1.086e+02	1.557e-01
0.70	0.80	1.178e+02	1.296e-01
0.80	0.80	1.242e+02	1.142e-01
0.90	0.80	1.284e+02	1.053e-01
1.00	0.80	1.313e+02	1.001e-01
1.10	0.80	1.333e+02	9.681e-02
1.20	0.80	1.347e+02	9.465e-02
1.30	0.80	1.358e+02	9.314e-02
1.40	0.80	1.366e+02	9.201e-02
1.50	0.80	1.373e+02	9.112e-02

Table 6. Id and Ig vs. Vds (Vgs stepped) for d125 DHFET Simulation at 125C (page 6).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
1.60	0.80	1.379e+02	9.039e-02
1.70	0.80	1.384e+02	8.977e-02
1.80	0.80	1.388e+02	8.922e-02
1.90	0.80	1.392e+02	8.872e-02
2.00	0.80	1.396e+02	8.827e-02
2.10	0.80	1.400e+02	8.785e-02
2.20	0.80	1.403e+02	8.746e-02
2.30	0.80	1.406e+02	8.708e-02
2.40	0.80	1.409e+02	8.672e-02
2.50	0.80	1.412e+02	8.638e-02
0.00	1.00	-2.749e+00	5.498e+00
0.10	1.00	2.118e+01	3.755e+00
0.20	1.00	4.415e+01	2.578e+00
0.30	1.00	6.596e+01	1.789e+00
0.40	1.00	8.627e+01	1.262e+00
0.50	1.00	1.046e+02	9.134e-01
0.60	1.00	1.202e+02	6.870e-01
0.70	1.00	1.327e+02	5.440e-01
0.80	1.00	1.420e+02	4.569e-01
0.90	1.00	1.484e+02	4.054e-01
1.00	1.00	1.527e+02	3.752e-01
1.10	1.00	1.556e+02	3.570e-01
1.20	1.00	1.576e+02	3.455e-01
1.30	1.00	1.591e+02	3.379e-01
1.40	1.00	1.602e+02	3.324e-01
1.50	1.00	1.611e+02	3.284e-01
1.60	1.00	1.618e+02	3.251e-01
1.70	1.00	1.624e+02	3.225e-01
1.80	1.00	1.630e+02	3.202e-01
1.90	1.00	1.634e+02	3.182e-01
2.00	1.00	1.638e+02	3.165e-01
2.10	1.00	1.642e+02	3.149e-01
2.20	1.00	1.646e+02	3.134e-01
2.30	1.00	1.649e+02	3.120e-01
2.40	1.00	1.652e+02	3.106e-01
2.50	1.00	1.655e+02	3.094e-01

Table 7. Id and Ig vs. Vgs (Vds stepped) for d125 DHFET Simulation at 125C.

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
0.20	-1.00	1.335e-03	-2.046e-03
0.20	-0.90	1.544e-03	-2.045e-03
0.20	-0.80	2.069e-03	-2.043e-03
0.20	-0.70	4.107e-03	-2.040e-03
0.20	-0.60	3.872e-02	-2.034e-03
0.20	-0.50	4.647e+00	-2.022e-03
0.20	-0.40	9.942e+00	-1.997e-03
0.20	-0.30	1.473e+01	-1.942e-03
0.20	-0.20	1.901e+01	-1.826e-03
0.20	-0.10	2.282e+01	-1.574e-03
0.20	0.00	2.619e+01	-1.026e-03
0.20	0.10	2.917e+01	1.689e-04
0.20	0.20	3.181e+01	2.784e-03
0.20	0.30	3.416e+01	8.515e-03
0.20	0.40	3.626e+01	2.110e-02
0.20	0.50	3.814e+01	4.874e-02
0.20	0.60	3.982e+01	1.095e-01
0.20	0.70	4.131e+01	2.431e-01
0.20	0.80	4.260e+01	5.367e-01
0.20	0.90	4.360e+01	1.180e+00
0.20	1.00	4.415e+01	2.578e+00
0.40	-1.00	3.478e-03	-2.046e-03
0.40	-0.90	5.123e-03	-2.046e-03
0.40	-0.80	9.215e-03	-2.044e-03
0.40	-0.70	2.480e-02	-2.041e-03
0.40	-0.60	2.313e-01	-2.036e-03
0.40	-0.50	6.420e+00	-2.026e-03
0.40	-0.40	1.384e+01	-2.007e-03
0.40	-0.30	2.114e+01	-1.967e-03
0.40	-0.20	2.827e+01	-1.888e-03
0.40	-0.10	3.516e+01	-1.724e-03
0.40	0.00	4.177e+01	-1.384e-03
0.40	0.10	4.804e+01	-6.745e-04
0.40	0.20	5.392e+01	8.165e-04
0.40	0.30	5.939e+01	3.972e-03
0.40	0.40	6.444e+01	1.069e-02
0.40	0.50	6.906e+01	2.509e-02
0.40	0.60	7.327e+01	5.606e-02
0.40	0.70	7.709e+01	1.229e-01
0.40	0.80	8.055e+01	2.678e-01
0.40	0.90	8.363e+01	5.819e-01
0.40	1.00	8.627e+01	1.262e+00
0.60	-1.00	9.212e-03	-2.047e-03
0.60	-0.90	1.466e-02	-2.046e-03
0.60	-0.80	2.810e-02	-2.045e-03
0.60	-0.70	7.767e-02	-2.042e-03
0.60	-0.60	5.685e-01	-2.037e-03
0.60	-0.50	7.302e+00	-2.027e-03
0.60	-0.40	1.540e+01	-2.010e-03
0.60	-0.30	2.355e+01	-1.974e-03

Table 7. Id and Ig vs. Vgs (Vds stepped) for d125 DHFET Simulation at 125C (page 2).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
0.60	-0.20	3.175e+01	-1.905e-03
0.60	-0.10	3.997e+01	-1.766e-03
0.60	0.00	4.820e+01	-1.490e-03
0.60	0.10	5.638e+01	-9.386e-04
0.60	0.20	6.450e+01	1.681e-04
0.60	0.30	7.249e+01	2.398e-03
0.60	0.40	8.031e+01	6.918e-03
0.60	0.50	8.790e+01	1.613e-02
0.60	0.60	9.518e+01	3.506e-02
0.60	0.70	1.021e+02	7.420e-02
0.60	0.80	1.086e+02	1.557e-01
0.60	0.90	1.147e+02	3.267e-01
0.60	1.00	1.202e+02	6.870e-01
0.80	-1.00	2.022e-02	-2.047e-03
0.80	-0.90	3.288e-02	-2.046e-03
0.80	-0.80	6.369e-02	-2.045e-03
0.80	-0.70	1.727e-01	-2.042e-03
0.80	-0.60	9.909e-01	-2.037e-03
0.80	-0.50	7.948e+00	-2.028e-03
0.80	-0.40	1.631e+01	-2.011e-03
0.80	-0.30	2.478e+01	-1.977e-03
0.80	-0.20	3.337e+01	-1.910e-03
0.80	-0.10	4.209e+01	-1.779e-03
0.80	0.00	5.091e+01	-1.523e-03
0.80	0.10	5.985e+01	-1.019e-03
0.80	0.20	6.889e+01	-3.166e-05
0.80	0.30	7.803e+01	1.906e-03
0.80	0.40	8.724e+01	5.707e-03
0.80	0.50	9.650e+01	1.317e-02
0.80	0.60	1.058e+02	2.786e-02
0.80	0.70	1.150e+02	5.684e-02
0.80	0.80	1.242e+02	1.142e-01
0.80	0.90	1.332e+02	2.284e-01
0.80	1.00	1.420e+02	4.569e-01
1.00	-1.00	3.809e-02	-2.048e-03
1.00	-0.90	6.225e-02	-2.047e-03
1.00	-0.80	1.201e-01	-2.046e-03
1.00	-0.70	3.150e-01	-2.043e-03
1.00	-0.60	1.459e+00	-2.038e-03
1.00	-0.50	8.514e+00	-2.029e-03
1.00	-0.40	1.699e+01	-2.012e-03
1.00	-0.30	2.561e+01	-1.978e-03
1.00	-0.20	3.438e+01	-1.913e-03
1.00	-0.10	4.330e+01	-1.785e-03
1.00	0.00	5.238e+01	-1.536e-03
1.00	0.10	6.162e+01	-1.050e-03
1.00	0.20	7.104e+01	-1.055e-04
1.00	0.30	8.063e+01	1.729e-03
1.00	0.40	9.040e+01	5.284e-03
1.00	0.50	1.003e+02	1.216e-02

Table 7. Id and Ig vs. Vgs (Vds stepped) for d125 DHFET Simulation at 125C (page 3).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
1.00	0.60	1.105e+02	2.542e-02
1.00	0.70	1.208e+02	5.096e-02
1.00	0.80	1.313e+02	1.001e-01
1.00	0.90	1.419e+02	1.944e-01
1.00	1.00	1.527e+02	3.752e-01
1.20	-1.00	6.432e-02	-2.048e-03
1.20	-0.90	1.050e-01	-2.047e-03
1.20	-0.80	2.006e-01	-2.046e-03
1.20	-0.70	5.053e-01	-2.043e-03
1.20	-0.60	1.952e+00	-2.038e-03
1.20	-0.50	9.047e+00	-2.029e-03
1.20	-0.40	1.759e+01	-2.012e-03
1.20	-0.30	2.629e+01	-1.979e-03
1.20	-0.20	3.514e+01	-1.915e-03
1.20	-0.10	4.416e+01	-1.789e-03
1.20	0.00	5.336e+01	-1.544e-03
1.20	0.10	6.275e+01	-1.067e-03
1.20	0.20	7.233e+01	-1.427e-04
1.20	0.30	8.213e+01	1.645e-03
1.20	0.40	9.214e+01	5.093e-03
1.20	0.50	1.024e+02	1.172e-02
1.20	0.60	1.129e+02	2.441e-02
1.20	0.70	1.236e+02	4.863e-02
1.20	0.80	1.347e+02	9.465e-02
1.20	0.90	1.460e+02	1.817e-01
1.20	1.00	1.576e+02	3.455e-01
1.40	-1.00	1.002e-01	-2.049e-03
1.40	-0.90	1.629e-01	-2.048e-03
1.40	-0.80	3.073e-01	-2.046e-03
1.40	-0.70	7.412e-01	-2.044e-03
1.40	-0.60	2.459e+00	-2.039e-03
1.40	-0.50	9.564e+00	-2.030e-03
1.40	-0.40	1.815e+01	-2.013e-03
1.40	-0.30	2.689e+01	-1.980e-03
1.40	-0.20	3.579e+01	-1.916e-03
1.40	-0.10	4.487e+01	-1.792e-03
1.40	0.00	5.414e+01	-1.549e-03
1.40	0.10	6.360e+01	-1.079e-03
1.40	0.20	7.327e+01	-1.675e-04
1.40	0.30	8.316e+01	1.592e-03
1.40	0.40	9.330e+01	4.978e-03
1.40	0.50	1.037e+02	1.147e-02
1.40	0.60	1.144e+02	2.387e-02
1.40	0.70	1.253e+02	4.744e-02
1.40	0.80	1.366e+02	9.201e-02
1.40	0.90	1.482e+02	1.758e-01
1.40	1.00	1.602e+02	3.524e-01
1.60	-1.00	1.471e-01	-2.049e-03
1.60	-0.90	2.377e-01	-2.048e-03
1.60	-0.80	4.415e-01	-2.047e-03

Table 7. Id and Ig vs. Vgs (Vds stepped) for d125 DHFET Simulation at 125C (page 4).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
1.60	-0.70	1.019e+00	-2.044e-03
1.60	-0.60	2.975e+00	-2.039e-03
1.60	-0.50	1.007e+01	-2.031e-03
1.60	-0.40	1.868e+01	-2.014e-03
1.60	-0.30	2.745e+01	-1.981e-03
1.60	-0.20	3.638e+01	-1.918e-03
1.60	-0.10	4.549e+01	-1.794e-03
1.60	0.00	5.480e+01	-1.554e-03
1.60	0.10	6.430e+01	-1.088e-03
1.60	0.20	7.403e+01	-1.869e-04
1.60	0.30	8.398e+01	1.552e-03
1.60	0.40	9.418e+01	4.895e-03
1.60	0.50	1.046e+02	1.130e-02
1.60	0.60	1.154e+02	2.350e-02
1.60	0.70	1.265e+02	4.667e-02
1.60	0.80	1.379e+02	9.039e-02
1.60	0.90	1.497e+02	1.724e-01
1.60	1.00	1.618e+02	3.251e-01
1.80	-1.00	2.059e-01	-2.050e-03
1.80	-0.90	3.304e-01	-2.049e-03
1.80	-0.80	6.036e-01	-2.047e-03
1.80	-0.70	1.333e+00	-2.045e-03
1.80	-0.60	3.496e+00	-2.040e-03
1.80	-0.50	1.057e+01	-2.031e-03
1.80	-0.40	1.920e+01	-2.014e-03
1.80	-0.30	2.798e+01	-1.982e-03
1.80	-0.20	3.694e+01	-1.919e-03
1.80	-0.10	4.607e+01	-1.797e-03
1.80	0.00	5.540e+01	-1.558e-03
1.80	0.10	6.493e+01	-1.097e-03
1.80	0.20	7.468e+01	-2.036e-04
1.80	0.30	8.467e+01	1.518e-03
1.80	0.40	9.491e+01	4.827e-03
1.80	0.50	1.054e+02	1.116e-02
1.80	0.60	1.162e+02	2.322e-02
1.80	0.70	1.274e+02	4.609e-02
1.80	0.80	1.388e+02	8.922e-02
1.80	0.90	1.507e+02	1.700e-01
1.80	1.00	1.630e+02	3.202e-01
2.00	-1.00	2.776e-01	-2.050e-03
2.00	-0.90	4.419e-01	-2.049e-03
2.00	-0.80	7.934e-01	-2.048e-03
2.00	-0.70	1.679e+00	-2.045e-03
2.00	-0.60	4.022e+00	-2.041e-03
2.00	-0.50	1.107e+01	-2.032e-03
2.00	-0.40	1.971e+01	-2.015e-03
2.00	-0.30	2.850e+01	-1.983e-03
2.00	-0.20	3.747e+01	-1.920e-03
2.00	-0.10	4.662e+01	-1.799e-03
2.00	0.00	5.597e+01	-1.563e-03

Table 7. Id and Ig vs. Vgs (Vds stepped) for d125 DHFET Simulation at 125C (page 5).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.00	0.10	6.552e+01	-1.105e-03
2.00	0.20	7.529e+01	-2.189e-04
2.00	0.30	8.530e+01	1.488e-03
2.00	0.40	9.556e+01	4.767e-03
2.00	0.50	1.061e+02	1.104e-02
2.00	0.60	1.169e+02	2.298e-02
2.00	0.70	1.281e+02	4.562e-02
2.00	0.80	1.396e+02	8.827e-02
2.00	0.90	1.515e+02	1.681e-01
2.00	1.00	1.638e+02	3.165e-01
2.20	-1.00	3.629e-01	-2.051e-03
2.20	-0.90	5.728e-01	-2.050e-03
2.20	-0.80	1.010e+00	-2.048e-03
2.20	-0.70	2.052e+00	-2.046e-03
2.20	-0.60	4.550e+00	-2.041e-03
2.20	-0.50	1.157e+01	-2.032e-03
2.20	-0.40	2.021e+01	-2.016e-03
2.20	-0.30	2.902e+01	-1.984e-03
2.20	-0.20	3.799e+01	-1.922e-03
2.20	-0.10	4.715e+01	-1.801e-03
2.20	0.00	5.651e+01	-1.567e-03
2.20	0.10	6.607e+01	-1.112e-03
2.20	0.20	7.585e+01	-2.331e-04
2.20	0.30	8.588e+01	1.461e-03
2.20	0.40	9.616e+01	4.713e-03
2.20	0.50	1.067e+02	1.093e-02
2.20	0.60	1.176e+02	2.277e-02
2.20	0.70	1.287e+02	4.520e-02
2.20	0.80	1.403e+02	8.746e-02
2.20	0.90	1.522e+02	1.665e-01
2.20	1.00	1.646e+02	3.134e-01
2.40	-1.00	4.624e-01	-2.051e-03
2.40	-0.90	7.234e-01	-2.050e-03
2.40	-0.80	1.252e+00	-2.049e-03
2.40	-0.70	2.448e+00	-2.046e-03
2.40	-0.60	5.080e+00	-2.042e-03
2.40	-0.50	1.207e+01	-2.033e-03
2.40	-0.40	2.071e+01	-2.016e-03
2.40	-0.30	2.952e+01	-1.985e-03
2.40	-0.20	3.851e+01	-1.923e-03
2.40	-0.10	4.767e+01	-1.803e-03
2.40	0.00	5.704e+01	-1.570e-03
2.40	0.10	6.661e+01	-1.119e-03
2.40	0.20	7.640e+01	-2.467e-04
2.40	0.30	8.643e+01	1.434e-03
2.40	0.40	9.672e+01	4.661e-03
2.40	0.50	1.073e+02	1.083e-02
2.40	0.60	1.182e+02	2.258e-02
2.40	0.70	1.293e+02	4.482e-02
2.40	0.80	1.409e+02	8.672e-02

Table 7. Id and Ig vs. Vgs (Vds stepped) for d125 DHFET Simulation at 125C (page 6).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.40	0.90	1.528e+02	1.651e-01
2.40	1.00	1.652e+02	3.106e-01

Table 8. I_g vs. V_{gs} ($V_{ds} = 0$) for d125 DHFET Simulation at 125C.

V_{gs} (V)	I_g ($\mu A/\mu m$)
0.00	-1.217e-10
0.02	3.513e-04
0.04	7.630e-04
0.06	1.245e-03
0.08	1.811e-03
0.10	2.473e-03
0.12	3.250e-03
0.14	4.160e-03
0.16	5.227e-03
0.18	6.477e-03
0.20	7.942e-03
0.22	9.659e-03
0.24	1.167e-02
0.26	1.403e-02
0.28	1.679e-02
0.30	2.003e-02
0.32	2.383e-02
0.34	2.828e-02
0.36	3.349e-02
0.38	3.960e-02
0.40	4.676e-02
0.42	5.515e-02
0.44	6.498e-02
0.46	7.650e-02
0.48	9.000e-02
0.50	1.058e-01
0.52	1.244e-01
0.54	1.461e-01
0.56	1.715e-01
0.58	2.013e-01
0.60	2.363e-01
0.62	2.772e-01
0.64	3.251e-01
0.66	3.812e-01
0.68	4.469e-01
0.70	5.239e-01
0.72	6.139e-01
0.74	7.194e-01
0.76	8.428e-01
0.78	9.871e-01
0.80	1.156e+00
0.82	1.353e+00
0.84	1.584e+00
0.86	1.853e+00
0.88	2.168e+00
0.90	2.535e+00
0.92	2.963e+00
0.94	3.461e+00
0.96	4.041e+00
0.98	4.715e+00

Table 8. I_g vs. V_{ds} ($V_{ds} = 0$) for d125 DHFET Simulation at 125C (page 2).

V_{gs} (V)	I_g ($\mu A/\mu m$)
1.00	5.498e+00
1.02	6.405e+00
1.04	7.454e+00
1.06	8.666e+00
1.08	1.006e+01
1.10	1.167e+01
1.12	1.351e+01
1.14	1.561e+01
1.16	1.801e+01
1.18	2.072e+01
1.20	2.380e+01
1.22	2.725e+01
1.24	3.112e+01
1.26	3.544e+01
1.28	4.023e+01
1.30	4.551e+01
1.32	5.132e+01
1.34	5.765e+01
1.36	6.453e+01
1.38	7.157e+01
1.40	7.996e+01
1.42	8.851e+01
1.44	9.762e+01
1.46	1.073e+02
1.48	1.174e+02
1.50	1.282e+02
1.52	1.394e+02
1.54	1.511e+02
1.56	1.632e+02
1.58	1.758e+02
1.60	1.889e+02

Table 9. Cgd and Cgs vs. Vds (Vgs stepped) for d125 DHFET Simulation at 125C.

Vds (V)	Vgs (V)	Cgd (fF/ μ m)	Cgs (fF/ μ m)
0.00	-1.00	2.604e-01	7.802e-01
0.50	-1.00	2.604e-01	7.802e-01
1.00	-1.00	2.604e-01	7.802e-01
1.50	-1.00	2.604e-01	7.802e-01
2.00	-1.00	2.604e-01	7.802e-01
2.50	-1.00	2.604e-01	7.802e-01
0.00	-0.75	2.604e-01	9.139e-01
0.50	-0.75	2.604e-01	9.139e-01
1.00	-0.75	2.604e-01	9.139e-01
1.50	-0.75	2.604e-01	9.139e-01
2.00	-0.75	2.604e-01	9.139e-01
2.50	-0.75	2.604e-01	9.139e-01
0.00	-0.50	2.604e-01	1.073e+00
0.50	-0.50	2.604e-01	1.073e+00
1.00	-0.50	2.604e-01	1.073e+00
1.50	-0.50	2.604e-01	1.073e+00
2.00	-0.50	2.604e-01	1.073e+00
2.50	-0.50	2.604e-01	1.073e+00
0.00	-0.25	2.604e-01	1.262e+00
0.50	-0.25	2.604e-01	1.262e+00
1.00	-0.25	2.604e-01	1.262e+00
1.50	-0.25	2.604e-01	1.262e+00
2.00	-0.25	2.604e-01	1.262e+00
2.50	-0.25	2.604e-01	1.262e+00
0.00	0.00	2.604e-01	1.487e+00
0.50	0.00	2.604e-01	1.487e+00
1.00	0.00	2.604e-01	1.487e+00
1.50	0.00	2.604e-01	1.487e+00
2.00	0.00	2.604e-01	1.487e+00
2.50	0.00	2.604e-01	1.487e+00
0.00	0.25	2.604e-01	1.756e+00
0.50	0.25	2.604e-01	1.756e+00
1.00	0.25	2.604e-01	1.756e+00
1.50	0.25	2.604e-01	1.756e+00
2.00	0.25	2.604e-01	1.756e+00
2.50	0.25	2.604e-01	1.756e+00
0.00	0.50	2.604e-01	2.078e+00
0.50	0.50	2.604e-01	2.078e+00
1.00	0.50	2.604e-01	2.078e+00
1.50	0.50	2.604e-01	2.078e+00
2.00	0.50	2.604e-01	2.078e+00
2.50	0.50	2.604e-01	2.078e+00
0.00	0.75	2.604e-01	2.465e+00
0.50	0.75	2.604e-01	2.465e+00
1.00	0.75	2.604e-01	2.465e+00
1.50	0.75	2.604e-01	2.465e+00
2.00	0.75	2.604e-01	2.465e+00
2.50	0.75	2.604e-01	2.465e+00

Table 10. Cgd and Cgs vs. Vgs (Vds stepped) for d125 DHFET Simulation at 125C.

Vds (V)	Vgs (V)	Cgd (fF/ μ m)	Cgs (fF/ μ m)
0.00	-1.00	2.604e-01	7.802e-01
0.00	-0.90	2.604e-01	8.310e-01
0.00	-0.80	2.604e-01	8.853e-01
0.00	-0.70	2.604e-01	9.435e-01
0.00	-0.60	2.604e-01	1.006e+00
0.00	-0.50	2.604e-01	1.073e+00
0.00	-0.40	2.604e-01	1.144e+00
0.00	-0.30	2.604e-01	1.221e+00
0.00	-0.20	2.604e-01	1.303e+00
0.00	-0.10	2.604e-01	1.392e+00
0.00	0.00	2.604e-01	1.487e+00
0.00	0.10	2.604e-01	1.589e+00
0.00	0.20	2.604e-01	1.698e+00
0.00	0.30	2.604e-01	1.816e+00
0.00	0.40	2.604e-01	1.942e+00
0.00	0.50	2.604e-01	2.078e+00
0.00	0.60	2.604e-01	2.224e+00
0.00	0.70	2.604e-01	2.382e+00
0.00	0.80	2.604e-01	2.552e+00
0.00	0.90	2.604e-01	2.734e+00
0.00	1.00	2.604e-01	2.931e+00
2.50	-1.00	2.604e-01	7.802e-01
2.50	-0.90	2.604e-01	8.310e-01
2.50	-0.80	2.604e-01	8.853e-01
2.50	-0.70	2.604e-01	9.435e-01
2.50	-0.60	2.604e-01	1.006e+00
2.50	-0.50	2.604e-01	1.073e+00
2.50	-0.40	2.604e-01	1.144e+00
2.50	-0.30	2.604e-01	1.221e+00
2.50	-0.20	2.604e-01	1.303e+00
2.50	-0.10	2.604e-01	1.392e+00
2.50	0.00	2.604e-01	1.487e+00
2.50	0.10	2.604e-01	1.589e+00
2.50	0.20	2.604e-01	1.698e+00
2.50	0.30	2.604e-01	1.816e+00
2.50	0.40	2.604e-01	1.942e+00
2.50	0.50	2.604e-01	2.078e+00
2.50	0.60	2.604e-01	2.224e+00
2.50	0.70	2.604e-01	2.382e+00
2.50	0.80	2.604e-01	2.552e+00
2.50	0.90	2.604e-01	2.734e+00
2.50	1.00	2.604e-01	2.931e+00

Table 11. Id and Ig vs. Vds (Vgs stepped) for e25 EHFET Simulation at 25C.

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
0.00	0.00	2.206e-11	-4.412e-11
0.10	0.00	4.425e-04	-3.006e-04
0.20	0.00	1.334e-03	-3.574e-04
0.30	0.00	3.382e-03	-3.682e-04
0.40	0.00	7.059e-03	-3.705e-04
0.50	0.00	1.276e-02	-3.711e-04
0.60	0.00	2.084e-02	-3.714e-04
0.70	0.00	3.161e-02	-3.717e-04
0.80	0.00	4.536e-02	-3.720e-04
0.90	0.00	6.232e-02	-3.724e-04
1.00	0.00	8.272e-02	-3.727e-04
1.10	0.00	1.067e-01	-3.731e-04
1.20	0.00	1.346e-01	-3.735e-04
1.30	0.00	1.663e-01	-3.739e-04
1.40	0.00	2.021e-01	-3.744e-04
1.50	0.00	2.420e-01	-3.749e-04
1.60	0.00	2.861e-01	-3.754e-04
1.70	0.00	3.344e-01	-3.759e-04
1.80	0.00	3.870e-01	-3.765e-04
1.90	0.00	4.439e-01	-3.771e-04
2.00	0.00	5.050e-01	-3.777e-04
2.10	0.00	5.704e-01	-3.783e-04
2.20	0.00	6.400e-01	-3.790e-04
2.30	0.00	7.137e-01	-3.797e-04
2.40	0.00	7.916e-01	-3.804e-04
2.50	0.00	8.735e-01	-3.812e-04
0.00	0.10	-1.594e-03	3.188e-03
0.10	0.10	4.539e-04	1.594e-03
0.20	0.10	3.410e-03	1.293e-03
0.30	0.10	9.881e-03	1.236e-03
0.40	0.10	2.132e-02	1.225e-03
0.50	0.10	3.876e-02	1.222e-03
0.60	0.10	6.302e-02	1.221e-03
0.70	0.10	9.468e-02	1.220e-03
0.80	0.10	1.341e-01	1.218e-03
0.90	0.10	1.817e-01	1.216e-03
1.00	0.10	2.374e-01	1.214e-03
1.10	0.10	3.013e-01	1.212e-03
1.20	0.10	3.733e-01	1.209e-03
1.30	0.10	4.531e-01	1.206e-03
1.40	0.10	5.406e-01	1.203e-03
1.50	0.10	6.354e-01	1.199e-03
1.60	0.10	7.373e-01	1.196e-03
1.70	0.10	8.458e-01	1.192e-03
1.80	0.10	9.608e-01	1.188e-03
1.90	0.10	1.082e+00	1.184e-03
2.00	0.10	1.208e+00	1.179e-03
2.10	0.10	1.340e+00	1.175e-03
2.20	0.10	1.477e+00	1.170e-03
2.30	0.10	1.618e+00	1.165e-03

Table 11. Id and Ig vs. Vds (Vgs stepped) for e25 EHFET Simulation at 25C (page 2).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.40	0.10	1.764e+00	1.160e-03
2.50	0.10	1.914e+00	1.155e-03
0.00	0.20	-1.005e-02	2.010e-02
0.10	0.20	3.079e-02	1.164e-02
0.20	0.20	1.513e-01	1.002e-02
0.30	0.20	3.209e-01	9.692e-03
0.40	0.20	5.122e-01	9.601e-03
0.50	0.20	7.136e-01	9.554e-03
0.60	0.20	9.203e-01	9.515e-03
0.70	0.20	1.130e+00	9.477e-03
0.80	0.20	1.341e+00	9.440e-03
0.90	0.20	1.554e+00	9.402e-03
1.00	0.20	1.767e+00	9.365e-03
1.10	0.20	1.981e+00	9.327e-03
1.20	0.20	2.195e+00	9.290e-03
1.30	0.20	2.410e+00	9.252e-03
1.40	0.20	2.624e+00	9.215e-03
1.50	0.20	2.839e+00	9.178e-03
1.60	0.20	3.054e+00	9.141e-03
1.70	0.20	3.269e+00	9.104e-03
1.80	0.20	3.485e+00	9.067e-03
1.90	0.20	3.700e+00	9.030e-03
2.00	0.20	3.915e+00	8.994e-03
2.10	0.20	4.130e+00	8.957e-03
2.20	0.20	4.346e+00	8.921e-03
2.30	0.20	4.561e+00	8.885e-03
2.40	0.20	4.777e+00	8.849e-03
2.50	0.20	4.992e+00	8.813e-03
0.00	0.30	-5.478e-02	1.096e-01
0.10	0.30	6.926e+00	5.996e-02
0.20	0.30	1.056e+01	4.761e-02
0.30	0.30	1.230e+01	4.436e-02
0.40	0.30	1.324e+01	4.327e-02
0.50	0.30	1.383e+01	4.275e-02
0.60	0.30	1.427e+01	4.241e-02
0.70	0.30	1.461e+01	4.215e-02
0.80	0.30	1.491e+01	4.193e-02
0.90	0.30	1.518e+01	4.173e-02
1.00	0.30	1.543e+01	4.155e-02
1.10	0.30	1.566e+01	4.138e-02
1.20	0.30	1.588e+01	4.122e-02
1.30	0.30	1.610e+01	4.106e-02
1.40	0.30	1.631e+01	4.091e-02
1.50	0.30	1.652e+01	4.076e-02
1.60	0.30	1.673e+01	4.061e-02
1.70	0.30	1.693e+01	4.046e-02
1.80	0.30	1.714e+01	4.032e-02
1.90	0.30	1.734e+01	4.017e-02
2.00	0.30	1.754e+01	4.003e-02
2.10	0.30	1.774e+01	3.989e-02

Table 11. Id and Ig vs. Vds (Vgs stepped) for e25 EHFET Simulation at 25C (page 3).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.20	0.30	1.793e+01	3.975e-02
2.30	0.30	1.813e+01	3.962e-02
2.40	0.30	1.833e+01	3.948e-02
2.50	0.30	1.852e+01	3.934e-02
0.00	0.40	-2.887e-01	5.774e-01
0.10	0.40	1.281e+01	3.006e-01
0.20	0.40	2.059e+01	2.180e-01
0.30	0.40	2.448e+01	1.931e-01
0.40	0.40	2.647e+01	1.843e-01
0.50	0.40	2.763e+01	1.802e-01
0.60	0.40	2.838e+01	1.778e-01
0.70	0.40	2.893e+01	1.761e-01
0.80	0.40	2.936e+01	1.748e-01
0.90	0.40	2.972e+01	1.737e-01
1.00	0.40	3.003e+01	1.728e-01
1.10	0.40	3.031e+01	1.719e-01
1.20	0.40	3.057e+01	1.711e-01
1.30	0.40	3.082e+01	1.704e-01
1.40	0.40	3.106e+01	1.697e-01
1.50	0.40	3.128e+01	1.691e-01
1.60	0.40	3.150e+01	1.684e-01
1.70	0.40	3.172e+01	1.678e-01
1.80	0.40	3.193e+01	1.672e-01
1.90	0.40	3.214e+01	1.666e-01
2.00	0.40	3.235e+01	1.660e-01
2.10	0.40	3.255e+01	1.654e-01
2.20	0.40	3.275e+01	1.648e-01
2.30	0.40	3.295e+01	1.642e-01
2.40	0.40	3.315e+01	1.637e-01
2.50	0.40	3.335e+01	1.631e-01
0.00	0.50	-1.442e+00	2.883e+00
0.10	0.50	1.738e+01	1.479e+00
0.20	0.50	2.979e+01	9.885e-01
0.30	0.50	3.649e+01	8.232e-01
0.40	0.50	3.994e+01	7.627e-01
0.50	0.50	4.186e+01	7.355e-01
0.60	0.50	4.304e+01	7.204e-01
0.70	0.50	4.384e+01	7.106e-01
0.80	0.50	4.444e+01	7.034e-01
0.90	0.50	4.491e+01	6.979e-01
1.00	0.50	4.530e+01	6.933e-01
1.10	0.50	4.564e+01	6.893e-01
1.20	0.50	4.594e+01	6.857e-01
1.30	0.50	4.622e+01	6.825e-01
1.40	0.50	4.649e+01	6.795e-01
1.50	0.50	4.673e+01	6.766e-01
1.60	0.50	4.697e+01	6.739e-01
1.70	0.50	4.720e+01	6.713e-01
1.80	0.50	4.742e+01	6.688e-01
1.90	0.50	4.764e+01	6.663e-01

Table 11. Id and Ig vs. Vds (Vgs stepped) for e25 EHFET Simulation at 25C (page 4).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.00	0.50	4.786e+01	6.639e-01
2.10	0.50	4.807e+01	6.616e-01
2.20	0.50	4.827e+01	6.592e-01
2.30	0.50	4.848e+01	6.569e-01
2.40	0.50	4.868e+01	6.547e-01
2.50	0.50	4.889e+01	6.524e-01
0.00	0.60	-5.993e+00	1.199e+01
0.10	0.60	1.936e+01	6.608e+00
0.20	0.60	3.722e+01	4.250e+00
0.30	0.60	4.767e+01	3.337e+00
0.40	0.60	5.318e+01	2.986e+00
0.50	0.60	5.617e+01	2.832e+00
0.60	0.60	5.793e+01	2.751e+00
0.70	0.60	5.908e+01	2.701e+00
0.80	0.60	5.989e+01	2.667e+00
0.90	0.60	6.050e+01	2.641e+00
1.00	0.60	6.099e+01	2.621e+00
1.10	0.60	6.140e+01	2.604e+00
1.20	0.60	6.176e+01	2.589e+00
1.30	0.60	6.208e+01	2.576e+00
1.40	0.60	6.237e+01	2.564e+00
1.50	0.60	6.264e+01	2.553e+00
1.60	0.60	6.290e+01	2.542e+00
1.70	0.60	6.315e+01	2.533e+00
1.80	0.60	6.339e+01	2.523e+00
1.90	0.60	6.361e+01	2.514e+00
2.00	0.60	6.384e+01	2.505e+00
2.10	0.60	6.406e+01	2.496e+00
2.20	0.60	6.427e+01	2.488e+00
2.30	0.60	6.448e+01	2.479e+00
2.40	0.60	6.469e+01	2.471e+00
2.50	0.60	6.490e+01	2.463e+00
0.00	0.70	-1.732e+01	3.464e+01
0.10	0.70	1.541e+01	2.238e+01
0.20	0.70	4.017e+01	1.516e+01
0.30	0.70	5.591e+01	1.165e+01
0.40	0.70	6.457e+01	1.015e+01
0.50	0.70	6.919e+01	9.489e+00
0.60	0.70	7.182e+01	9.153e+00
0.70	0.70	7.345e+01	8.956e+00
0.80	0.70	7.456e+01	8.826e+00
0.90	0.70	7.537e+01	8.732e+00
1.00	0.70	7.599e+01	8.660e+00
1.10	0.70	7.650e+01	8.602e+00
1.20	0.70	7.693e+01	8.553e+00
1.30	0.70	7.731e+01	8.510e+00
1.40	0.70	7.765e+01	8.472e+00
1.50	0.70	7.796e+01	8.437e+00
1.60	0.70	7.824e+01	8.405e+00
1.70	0.70	7.851e+01	8.375e+00

Table 11. Id and Ig vs. Vds (Vgs stepped) for e25 EHFET Simulation at 25C (page 5).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
1.80	0.70	7.877e+01	8.346e+00
1.90	0.70	7.902e+01	8.318e+00
2.00	0.70	7.926e+01	8.291e+00
2.10	0.70	7.950e+01	8.265e+00
2.20	0.70	7.972e+01	8.240e+00
2.30	0.70	7.995e+01	8.216e+00
2.40	0.70	8.017e+01	8.191e+00
2.50	0.70	8.039e+01	8.167e+00
0.00	0.80	-3.520e+01	7.040e+01
0.10	0.80	3.680e+00	5.227e+01
0.20	0.80	3.544e+01	3.905e+01
0.30	0.80	5.767e+01	3.098e+01
0.40	0.80	7.070e+01	2.694e+01
0.50	0.80	7.765e+01	2.508e+01
0.60	0.80	8.146e+01	2.415e+01
0.70	0.80	8.374e+01	2.363e+01
0.80	0.80	8.523e+01	2.330e+01
0.90	0.80	8.629e+01	2.307e+01
1.00	0.80	8.708e+01	2.289e+01
1.10	0.80	8.771e+01	2.275e+01
1.20	0.80	8.823e+01	2.264e+01
1.30	0.80	8.867e+01	2.255e+01
1.40	0.80	8.907e+01	2.246e+01
1.50	0.80	8.942e+01	2.238e+01
1.60	0.80	8.975e+01	2.231e+01
1.70	0.80	9.005e+01	2.225e+01
1.80	0.80	9.034e+01	2.219e+01
1.90	0.80	9.061e+01	2.213e+01
2.00	0.80	9.088e+01	2.207e+01
2.10	0.80	9.113e+01	2.202e+01
2.20	0.80	9.138e+01	2.196e+01
2.30	0.80	9.162e+01	2.191e+01
2.40	0.80	9.186e+01	2.186e+01
2.50	0.80	9.210e+01	2.181e+01
0.00	0.90	-5.724e+01	1.145e+02
0.10	0.90	-1.390e+01	9.264e+01
0.20	0.90	2.373e+01	7.475e+01
0.30	0.90	5.268e+01	6.189e+01
0.40	0.90	7.128e+01	5.433e+01
0.50	0.90	8.147e+01	5.058e+01
0.60	0.90	8.687e+01	4.877e+01
0.70	0.90	8.995e+01	4.779e+01
0.80	0.90	9.189e+01	4.719e+01
0.90	0.90	9.321e+01	4.679e+01
1.00	0.90	9.418e+01	4.649e+01
1.10	0.90	9.492e+01	4.627e+01
1.20	0.90	9.553e+01	4.608e+01
1.30	0.90	9.604e+01	4.593e+01
1.40	0.90	9.648e+01	4.580e+01
1.50	0.90	9.688e+01	4.568e+01

Table 11. Id and Ig vs. Vds (Vgs stepped) for e25 EHFET Simulation at 25C (page 6).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
1.60	0.90	9.724e+01	4.557e+01
1.70	0.90	9.757e+01	4.547e+01
1.80	0.90	9.788e+01	4.537e+01
1.90	0.90	9.818e+01	4.528e+01
2.00	0.90	9.846e+01	4.520e+01
2.10	0.90	9.874e+01	4.512e+01
2.20	0.90	9.900e+01	4.504e+01
2.30	0.90	9.926e+01	4.496e+01
2.40	0.90	9.951e+01	4.489e+01
2.50	0.90	9.976e+01	4.481e+01
0.00	1.00	-8.171e+01	1.634e+02
0.10	1.00	-3.515e+01	1.393e+02
0.20	1.00	6.964e+00	1.182e+02
0.30	1.00	4.194e+01	1.013e+02
0.40	1.00	6.690e+01	8.990e+01
0.50	1.00	8.157e+01	8.361e+01
0.60	1.00	8.926e+01	8.055e+01
0.70	1.00	9.342e+01	7.899e+01
0.80	1.00	9.590e+01	7.808e+01
0.90	1.00	9.753e+01	7.750e+01
1.00	1.00	9.868e+01	7.708e+01
1.10	1.00	9.956e+01	7.677e+01
1.20	1.00	1.002e+02	7.652e+01
1.30	1.00	1.008e+02	7.632e+01
1.40	1.00	1.013e+02	7.614e+01
1.50	1.00	1.017e+02	7.599e+01
1.60	1.00	1.021e+02	7.585e+01
1.70	1.00	1.025e+02	7.572e+01
1.80	1.00	1.028e+02	7.561e+01
1.90	1.00	1.031e+02	7.549e+01
2.00	1.00	1.034e+02	7.539e+01
2.10	1.00	1.037e+02	7.529e+01
2.20	1.00	1.040e+02	7.519e+01
2.30	1.00	1.043e+02	7.509e+01
2.40	1.00	1.045e+02	7.500e+01
2.50	1.00	1.048e+02	7.491e+01

Table 12. Id and Ig vs. Vgs (Vds stepped) for e25 EHFET Simulation at 25C.

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
0.20	-1.00	4.152e-04	-7.448e-04
0.20	-0.90	4.221e-04	-7.444e-04
0.20	-0.80	4.310e-04	-7.439e-04
0.20	-0.70	4.428e-04	-7.435e-04
0.20	-0.60	4.590e-04	-7.430e-04
0.20	-0.50	4.819e-04	-7.425e-04
0.20	-0.40	5.161e-04	-7.417e-04
0.20	-0.30	5.706e-04	-7.392e-04
0.20	-0.20	6.653e-04	-7.278e-04
0.20	-0.10	8.546e-04	-6.688e-04
0.20	0.00	1.334e-03	-3.574e-04
0.20	0.10	3.410e-03	1.293e-03
0.20	0.20	1.513e-01	1.002e-02
0.20	0.30	1.056e+01	4.761e-02
0.20	0.40	2.059e+01	2.180e-01
0.20	0.50	2.979e+01	9.885e-01
0.20	0.60	3.722e+01	4.250e+00
0.20	0.70	4.017e+01	1.516e+01
0.20	0.80	3.544e+01	3.905e+01
0.20	0.90	2.373e+01	7.475e+01
0.20	1.00	6.964e+00	1.182e+02
0.40	-1.00	6.666e-04	-7.453e-04
0.40	-0.90	7.153e-04	-7.448e-04
0.40	-0.80	7.780e-04	-7.444e-04
0.40	-0.70	8.607e-04	-7.439e-04
0.40	-0.60	9.734e-04	-7.435e-04
0.40	-0.50	1.133e-03	-7.430e-04
0.40	-0.40	1.370e-03	-7.422e-04
0.40	-0.30	1.746e-03	-7.397e-04
0.40	-0.20	2.401e-03	-7.286e-04
0.40	-0.10	3.713e-03	-6.716e-04
0.40	0.00	7.059e-03	-3.705e-04
0.40	0.10	2.132e-02	1.225e-03
0.40	0.20	5.122e-01	9.601e-03
0.40	0.30	1.324e+01	4.327e-02
0.40	0.40	2.647e+01	1.843e-01
0.40	0.50	3.994e+01	7.627e-01
0.40	0.60	5.318e+01	2.986e+00
0.40	0.70	6.457e+01	1.015e+01
0.40	0.80	7.070e+01	2.694e+01
0.40	0.90	7.128e+01	5.433e+01
0.40	1.00	6.690e+01	8.990e+01
0.60	-1.00	1.281e-03	-7.458e-04
0.60	-0.90	1.432e-03	-7.453e-04
0.60	-0.80	1.626e-03	-7.448e-04
0.60	-0.70	1.883e-03	-7.444e-04
0.60	-0.60	2.231e-03	-7.439e-04
0.60	-0.50	2.724e-03	-7.434e-04
0.60	-0.40	3.455e-03	-7.426e-04
0.60	-0.30	4.615e-03	-7.402e-04

Table 12. Id and Ig vs. Vgs (Vds stepped) for e25 EHFET Simulation at 25C (page 2).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
0.60	-0.20	6.631e-03	-7.291e-04
0.60	-0.10	1.066e-02	-6.721e-04
0.60	0.00	2.084e-02	-3.714e-04
0.60	0.10	6.302e-02	1.221e-03
0.60	0.20	9.203e-01	9.515e-03
0.60	0.30	1.427e+01	4.241e-02
0.60	0.40	2.838e+01	1.778e-01
0.60	0.50	4.304e+01	7.204e-01
0.60	0.60	5.793e+01	2.751e+00
0.60	0.70	7.182e+01	9.153e+00
0.60	0.80	8.146e+01	2.415e+01
0.60	0.90	8.687e+01	4.877e+01
0.60	1.00	8.926e+01	8.055e+01
0.80	-1.00	2.396e-03	-7.462e-04
0.80	-0.90	2.732e-03	-7.458e-04
0.80	-0.80	3.165e-03	-7.453e-04
0.80	-0.70	3.735e-03	-7.448e-04
0.80	-0.60	4.511e-03	-7.444e-04
0.80	-0.50	5.606e-03	-7.439e-04
0.80	-0.40	7.230e-03	-7.431e-04
0.80	-0.30	9.801e-03	-7.406e-04
0.80	-0.20	1.426e-02	-7.296e-04
0.80	-0.10	2.314e-02	-6.725e-04
0.80	0.00	4.536e-02	-3.720e-04
0.80	0.10	1.341e-01	1.218e-03
0.80	0.20	1.341e+00	9.440e-03
0.80	0.30	1.491e+01	4.193e-02
0.80	0.40	2.936e+01	1.748e-01
0.80	0.50	4.444e+01	7.034e-01
0.80	0.60	5.989e+01	2.667e+00
0.80	0.70	7.456e+01	8.826e+00
0.80	0.80	8.523e+01	2.330e+01
0.80	0.90	9.189e+01	4.719e+01
0.80	1.00	9.587e+01	7.809e+01
1.00	-1.00	4.136e-03	-7.467e-04
1.00	-0.90	4.762e-03	-7.462e-04
1.00	-0.80	5.566e-03	-7.458e-04
1.00	-0.70	6.626e-03	-7.453e-04
1.00	-0.60	8.066e-03	-7.448e-04
1.00	-0.50	1.010e-02	-7.444e-04
1.00	-0.40	1.311e-02	-7.435e-04
1.00	-0.30	1.787e-02	-7.411e-04
1.00	-0.20	2.610e-02	-7.300e-04
1.00	-0.10	4.240e-02	-6.730e-04
1.00	0.00	8.272e-02	-3.727e-04
1.00	0.10	2.374e-01	1.214e-03
1.00	0.20	1.767e+00	9.365e-03
1.00	0.30	1.543e+01	4.155e-02
1.00	0.40	3.003e+01	1.728e-01
1.00	0.50	4.530e+01	6.933e-01

Table 12. Id and Ig vs. Vgs (Vds stepped) for e25 EHFET Simulation at 25C (page 3).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
1.00	0.60	6.099e+01	2.621e+00
1.00	0.70	7.599e+01	8.660e+00
1.00	0.80	8.708e+01	2.289e+01
1.00	0.90	9.418e+01	4.650e+01
1.00	1.00	9.866e+01	7.709e+01
1.20	-1.00	6.621e-03	-7.471e-04
1.20	-0.90	7.659e-03	-7.467e-04
1.20	-0.80	8.992e-03	-7.462e-04
1.20	-0.70	1.075e-02	-7.458e-04
1.20	-0.60	1.313e-02	-7.453e-04
1.20	-0.50	1.650e-02	-7.448e-04
1.20	-0.40	2.147e-02	-7.440e-04
1.20	-0.30	2.933e-02	-7.416e-04
1.20	-0.20	4.287e-02	-7.305e-04
1.20	-0.10	6.951e-02	-6.735e-04
1.20	0.00	1.346e-01	-3.735e-04
1.20	0.10	3.733e-01	1.209e-03
1.20	0.20	2.195e+00	9.290e-03
1.20	0.30	1.588e+01	4.122e-02
1.20	0.40	3.057e+01	1.711e-01
1.20	0.50	4.594e+01	6.857e-01
1.20	0.60	6.176e+01	2.589e+00
1.20	0.70	7.693e+01	8.553e+00
1.20	0.80	8.823e+01	2.264e+01
1.20	0.90	9.553e+01	4.608e+01
1.20	1.00	1.002e+02	7.653e+01
1.40	-1.00	9.963e-03	-7.476e-04
1.40	-0.90	1.155e-02	-7.471e-04
1.40	-0.80	1.360e-02	-7.467e-04
1.40	-0.70	1.629e-02	-7.462e-04
1.40	-0.60	1.994e-02	-7.458e-04
1.40	-0.50	2.508e-02	-7.453e-04
1.40	-0.40	3.268e-02	-7.444e-04
1.40	-0.30	4.465e-02	-7.420e-04
1.40	-0.20	6.521e-02	-7.309e-04
1.40	-0.10	1.054e-01	-6.740e-04
1.40	0.00	2.021e-01	-3.744e-04
1.40	0.10	5.406e-01	1.203e-03
1.40	0.20	2.624e+00	9.215e-03
1.40	0.30	1.631e+01	4.091e-02
1.40	0.40	3.105e+01	1.697e-01
1.40	0.50	4.649e+01	6.795e-01
1.40	0.60	6.237e+01	2.564e+00
1.40	0.70	7.765e+01	8.472e+00
1.40	0.80	8.906e+01	2.246e+01
1.40	0.90	9.648e+01	4.580e+01
1.40	1.00	1.013e+02	7.615e+01
1.60	-1.00	1.427e-02	-7.480e-04
1.60	-0.90	1.657e-02	-7.476e-04
1.60	-0.80	1.952e-02	-7.471e-04

Table 12. Id and Ig vs. Vgs (Vds stepped) for e25 EHFET Simulation at 25C (page 4).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
1.60	-0.70	2.341e-02	-7.467e-04
1.60	-0.60	2.869e-02	-7.462e-04
1.60	-0.50	3.611e-02	-7.457e-04
1.60	-0.40	4.706e-02	-7.449e-04
1.60	-0.30	6.426e-02	-7.425e-04
1.60	-0.20	9.370e-02	-7.314e-04
1.60	-0.10	1.508e-01	-6.745e-04
1.60	0.00	2.861e-01	-3.754e-04
1.60	0.10	7.373e-01	1.196e-03
1.60	0.20	3.054e+00	9.141e-03
1.60	0.30	1.673e+01	4.061e-02
1.60	0.40	3.150e+01	1.684e-01
1.60	0.50	4.697e+01	6.739e-01
1.60	0.60	6.290e+01	2.542e+00
1.60	0.70	7.824e+01	8.405e+00
1.60	0.80	8.975e+01	2.231e+01
1.60	0.90	9.724e+01	4.557e+01
1.60	1.00	1.021e+02	7.586e+01
1.80	-1.00	1.964e-02	-7.485e-04
1.80	-0.90	2.283e-02	-7.480e-04
1.80	-0.80	2.692e-02	-7.476e-04
1.80	-0.70	3.230e-02	-7.471e-04
1.80	-0.60	3.958e-02	-7.467e-04
1.80	-0.50	4.983e-02	-7.462e-04
1.80	-0.40	6.492e-02	-7.454e-04
1.80	-0.30	8.856e-02	-7.429e-04
1.80	-0.20	1.288e-01	-7.319e-04
1.80	-0.10	2.064e-01	-6.750e-04
1.80	0.00	3.870e-01	-3.765e-04
1.80	0.10	9.608e-01	1.188e-03
1.80	0.20	3.485e+00	9.067e-03
1.80	0.30	1.714e+01	4.032e-02
1.80	0.40	3.193e+01	1.672e-01
1.80	0.50	4.742e+01	6.688e-01
1.80	0.60	6.339e+01	2.523e+00
1.80	0.70	7.877e+01	8.346e+00
1.80	0.80	9.034e+01	2.219e+01
1.80	0.90	9.788e+01	4.537e+01
1.80	1.00	1.028e+02	7.561e+01
2.00	-1.00	2.618e-02	-7.489e-04
2.00	-0.90	3.044e-02	-7.485e-04
2.00	-0.80	3.590e-02	-7.480e-04
2.00	-0.70	4.309e-02	-7.476e-04
2.00	-0.60	5.282e-02	-7.471e-04
2.00	-0.50	6.647e-02	-7.466e-04
2.00	-0.40	8.654e-02	-7.458e-04
2.00	-0.30	1.179e-01	-7.434e-04
2.00	-0.20	1.711e-01	-7.323e-04
2.00	-0.10	2.727e-01	-6.756e-04
2.00	0.00	5.050e-01	-3.777e-04

Table 12. Id and Ig vs. Vgs (Vds stepped) for e25 EHFET Simulation at 25C (page 5).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.00	0.10	1.208e+00	1.179e-03
2.00	0.20	3.915e+00	8.994e-03
2.00	0.30	1.754e+01	4.003e-02
2.00	0.40	3.235e+01	1.660e-01
2.00	0.50	4.786e+01	6.639e-01
2.00	0.60	6.384e+01	2.505e+00
2.00	0.70	7.926e+01	8.291e+00
2.00	0.80	9.088e+01	2.207e+01
2.00	0.90	9.846e+01	4.520e+01
2.00	1.00	1.034e+02	7.539e+01
2.20	-1.00	3.397e-02	-7.494e-04
2.20	-0.90	3.951e-02	-7.489e-04
2.20	-0.80	4.662e-02	-7.485e-04
2.20	-0.70	5.594e-02	-7.480e-04
2.20	-0.60	6.856e-02	-7.476e-04
2.20	-0.50	8.624e-02	-7.471e-04
2.20	-0.40	1.122e-01	-7.463e-04
2.20	-0.30	1.526e-01	-7.438e-04
2.20	-0.20	2.209e-01	-7.328e-04
2.20	-0.10	3.501e-01	-6.761e-04
2.20	0.00	6.400e-01	-3.790e-04
2.20	0.10	1.477e+00	1.170e-03
2.20	0.20	4.346e+00	8.921e-03
2.20	0.30	1.793e+01	3.975e-02
2.20	0.40	3.275e+01	1.648e-01
2.20	0.50	4.827e+01	6.592e-01
2.20	0.60	6.427e+01	2.488e+00
2.20	0.70	7.972e+01	8.240e+00
2.20	0.80	9.138e+01	2.196e+01
2.20	0.90	9.900e+01	4.504e+01
2.20	1.00	1.040e+02	7.519e+01
2.40	-1.00	4.312e-02	-7.499e-04
2.40	-0.90	5.016e-02	-7.494e-04
2.40	-0.80	5.917e-02	-7.489e-04
2.40	-0.70	7.100e-02	-7.485e-04
2.40	-0.60	8.698e-02	-7.480e-04
2.40	-0.50	1.093e-01	-7.475e-04
2.40	-0.40	1.421e-01	-7.467e-04
2.40	-0.30	1.930e-01	-7.443e-04
2.40	-0.20	2.784e-01	-7.333e-04
2.40	-0.10	4.387e-01	-6.767e-04
2.40	0.00	7.916e-01	-3.804e-04
2.40	0.10	1.764e+00	1.160e-03
2.40	0.20	4.777e+00	8.849e-03
2.40	0.30	1.833e+01	3.948e-02
2.40	0.40	3.315e+01	1.637e-01
2.40	0.50	4.868e+01	6.547e-01
2.40	0.60	6.469e+01	2.471e+00
2.40	0.70	8.017e+01	8.191e+00
2.40	0.80	9.186e+01	2.186e+01

Table 12. Id and Ig vs. Vgs (Vds stepped) for e25 EHFET Simulation at 25C (page 6).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.40	0.90	9.951e+01	4.489e+01
2.40	1.00	1.045e+02	7.501e+01

Table 13. I_g vs. V_{gs} ($V_{ds} = 0$) for e25 EHFET Simulation at 25C.

V_{gs} (V)	I_g ($\mu A/\mu m$)
0.00	-4.412e-11
0.02	2.934e-04
0.04	7.030e-04
0.06	1.275e-03
0.08	2.073e-03
0.10	3.188e-03
0.12	4.744e-03
0.14	6.917e-03
0.16	9.951e-03
0.18	1.418e-02
0.20	2.010e-02
0.22	2.835e-02
0.24	3.986e-02
0.26	5.592e-02
0.28	7.833e-02
0.30	1.096e-01
0.32	1.531e-01
0.34	2.137e-01
0.36	2.980e-01
0.38	4.151e-01
0.40	5.774e-01
0.42	8.016e-01
0.44	1.110e+00
0.46	1.533e+00
0.48	2.108e+00
0.50	2.883e+00
0.52	3.916e+00
0.54	5.272e+00
0.56	7.024e+00
0.58	9.241e+00
0.60	1.199e+01
0.62	1.531e+01
0.64	1.924e+01
0.66	2.378e+01
0.68	2.892e+01
0.70	3.464e+01
0.72	4.089e+01
0.74	4.764e+01
0.76	5.484e+01
0.78	6.244e+01
0.80	7.040e+01
0.82	7.869e+01
0.84	8.727e+01
0.86	9.612e+01
0.88	1.052e+02
0.90	1.145e+02
0.92	1.240e+02
0.94	1.336e+02
0.96	1.434e+02
0.98	1.533e+02

Table 13. I_g vs. V_{ds} ($V_{ds} = 0$) for e25 EHFET Simulation at 25C (page 2).

V_{gs} (V)	I_g ($\mu A/\mu m$)
1.00	1.634e+02
1.02	1.736e+02
1.04	1.839e+02
1.06	1.943e+02
1.08	2.048e+02
1.10	2.153e+02
1.12	2.260e+02
1.14	2.367e+02
1.16	2.475e+02
1.18	2.583e+02
1.20	2.692e+02
1.22	2.801e+02
1.24	2.912e+02
1.26	3.022e+02
1.28	3.133e+02
1.30	3.244e+02
1.32	3.356e+02
1.34	3.468e+02
1.36	3.581e+02
1.38	3.694e+02
1.40	3.807e+02
1.42	3.920e+02
1.44	4.034e+02
1.46	4.148e+02
1.48	4.262e+02
1.50	4.377e+02
1.52	4.491e+02
1.54	4.606e+02
1.56	4.722e+02
1.58	4.837e+02
1.60	4.953e+02

Table 14. Cgd and Cgs vs. Vds (Vgs stepped) for e25 EHFET Simulation at 25C.

Vds (V)	Vgs (V)	Cgd (fF/ μ m)	Cgs (fF/ μ m)
0.00	-1.00	2.861e-01	5.050e-01
0.50	-1.00	2.861e-01	5.050e-01
1.00	-1.00	2.861e-01	5.050e-01
1.50	-1.00	2.861e-01	5.050e-01
2.00	-1.00	2.861e-01	5.050e-01
2.50	-1.00	2.861e-01	5.050e-01
0.00	-0.75	2.861e-01	5.845e-01
0.50	-0.75	2.861e-01	5.845e-01
1.00	-0.75	2.861e-01	5.845e-01
1.50	-0.75	2.861e-01	5.845e-01
2.00	-0.75	2.861e-01	5.845e-01
2.50	-0.75	2.861e-01	5.845e-01
0.00	-0.50	2.861e-01	6.964e-01
0.50	-0.50	2.861e-01	6.964e-01
1.00	-0.50	2.861e-01	6.964e-01
1.50	-0.50	2.861e-01	6.964e-01
2.00	-0.50	2.861e-01	6.964e-01
2.50	-0.50	2.861e-01	6.964e-01
0.00	-0.25	2.861e-01	8.639e-01
0.50	-0.25	2.861e-01	8.639e-01
1.00	-0.25	2.861e-01	8.639e-01
1.50	-0.25	2.861e-01	8.639e-01
2.00	-0.25	2.861e-01	8.639e-01
2.50	-0.25	2.861e-01	8.639e-01
0.00	0.00	2.861e-01	1.137e+00
0.50	0.00	2.861e-01	1.137e+00
1.00	0.00	2.861e-01	1.137e+00
1.50	0.00	2.861e-01	1.137e+00
2.00	0.00	2.861e-01	1.137e+00
2.50	0.00	2.861e-01	1.137e+00
0.00	0.25	2.861e-01	1.646e+00
0.50	0.25	2.861e-01	1.646e+00
1.00	0.25	2.861e-01	1.646e+00
1.50	0.25	2.861e-01	1.646e+00
2.00	0.25	2.861e-01	1.646e+00
2.50	0.25	2.861e-01	1.646e+00
0.00	0.50	2.861e-01	2.858e+00
0.50	0.50	2.861e-01	2.858e+00
1.00	0.50	2.861e-01	2.858e+00
1.50	0.50	2.861e-01	2.858e+00
2.00	0.50	2.861e-01	2.858e+00
2.50	0.50	2.861e-01	2.858e+00
0.00	0.75	2.861e-01	8.067e+00
0.50	0.75	2.861e-01	8.067e+00
1.00	0.75	2.861e-01	8.067e+00
1.50	0.75	2.861e-01	8.067e+00
2.00	0.75	2.861e-01	8.067e+00
2.50	0.75	2.861e-01	8.067e+00

Table 15. Cgd and Cgs vs. Vgs (Vds stepped) for e25 EHFET Simulation at 25C.

Vds (V)	Vgs (V)	Cgd (fF/ μ m)	Cgs (fF/ μ m)
0.00	-1.00	2.861e-01	5.050e-01
0.00	-0.90	2.861e-01	5.338e-01
0.00	-0.80	2.861e-01	5.665e-01
0.00	-0.70	2.861e-01	6.037e-01
0.00	-0.60	2.861e-01	6.466e-01
0.00	-0.50	2.861e-01	6.964e-01
0.00	-0.40	2.861e-01	7.548e-01
0.00	-0.30	2.861e-01	8.241e-01
0.00	-0.20	2.861e-01	9.076e-01
0.00	-0.10	2.861e-01	1.010e+00
0.00	0.00	2.861e-01	1.137e+00
0.00	0.10	2.861e-01	1.299e+00
0.00	0.20	2.861e-01	1.513e+00
0.00	0.30	2.861e-01	1.804e+00
0.00	0.40	2.861e-01	2.220e+00
0.00	0.50	2.861e-01	2.858e+00
0.00	0.60	2.861e-01	3.932e+00
0.00	0.70	2.861e-01	6.051e+00
0.00	0.80	2.861e-01	1.074e+01
0.00	0.90	2.861e-01	1.386e+01
0.00	1.00	2.861e-01	1.426e+01
2.50	-1.00	2.861e-01	5.050e-01
2.50	-0.90	2.861e-01	5.338e-01
2.50	-0.80	2.861e-01	5.665e-01
2.50	-0.70	2.861e-01	6.037e-01
2.50	-0.60	2.861e-01	6.466e-01
2.50	-0.50	2.861e-01	6.964e-01
2.50	-0.40	2.861e-01	7.548e-01
2.50	-0.30	2.861e-01	8.241e-01
2.50	-0.20	2.861e-01	9.076e-01
2.50	-0.10	2.861e-01	1.010e+00
2.50	0.00	2.861e-01	1.137e+00
2.50	0.10	2.861e-01	1.299e+00
2.50	0.20	2.861e-01	1.513e+00
2.50	0.30	2.861e-01	1.804e+00
2.50	0.40	2.861e-01	2.220e+00
2.50	0.50	2.861e-01	2.858e+00
2.50	0.60	2.861e-01	3.932e+00
2.50	0.70	2.861e-01	6.051e+00
2.50	0.80	2.861e-01	1.074e+01
2.50	0.90	2.861e-01	1.386e+01
2.50	1.00	2.861e-01	1.426e+01

Table 16. Id and Ig vs. Vds (Vgs stepped) for e125 EHFET Simulation at 125C.

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
0.00	0.00	1.312e-10	-2.623e-10
0.10	0.00	1.937e-03	-1.782e-03
0.20	0.00	3.527e-03	-2.121e-03
0.30	0.00	7.274e-03	-2.186e-03
0.40	0.00	1.480e-02	-2.199e-03
0.50	0.00	2.754e-02	-2.203e-03
0.60	0.00	4.678e-02	-2.204e-03
0.70	0.00	7.367e-02	-2.206e-03
0.80	0.00	1.091e-01	-2.208e-03
0.90	0.00	1.539e-01	-2.210e-03
1.00	0.00	2.086e-01	-2.213e-03
1.10	0.00	2.734e-01	-2.217e-03
1.20	0.00	3.484e-01	-2.220e-03
1.30	0.00	4.337e-01	-2.225e-03
1.40	0.00	5.289e-01	-2.230e-03
1.50	0.00	6.338e-01	-2.235e-03
1.60	0.00	7.480e-01	-2.241e-03
1.70	0.00	8.709e-01	-2.247e-03
1.80	0.00	1.002e+00	-2.253e-03
1.90	0.00	1.141e+00	-2.260e-03
2.00	0.00	1.287e+00	-2.267e-03
2.10	0.00	1.440e+00	-2.274e-03
2.20	0.00	1.599e+00	-2.282e-03
2.30	0.00	1.764e+00	-2.290e-03
2.40	0.00	1.934e+00	-2.298e-03
2.50	0.00	2.108e+00	-2.306e-03
0.00	0.10	-9.345e-03	1.869e-02
0.10	0.10	2.034e-03	9.346e-03
0.20	0.10	1.947e-02	7.561e-03
0.30	0.10	6.161e-02	7.211e-03
0.40	0.10	1.359e-01	7.128e-03
0.50	0.10	2.424e-01	7.089e-03
0.60	0.10	3.770e-01	7.053e-03
0.70	0.10	5.341e-01	7.014e-03
0.80	0.10	7.087e-01	6.971e-03
0.90	0.10	8.964e-01	6.925e-03
1.00	0.10	1.094e+00	6.876e-03
1.10	0.10	1.299e+00	6.826e-03
1.20	0.10	1.510e+00	6.775e-03
1.30	0.10	1.725e+00	6.723e-03
1.40	0.10	1.944e+00	6.671e-03
1.50	0.10	2.165e+00	6.618e-03
1.60	0.10	2.389e+00	6.565e-03
1.70	0.10	2.614e+00	6.512e-03
1.80	0.10	2.840e+00	6.458e-03
1.90	0.10	3.067e+00	6.405e-03
2.00	0.10	3.296e+00	6.352e-03
2.10	0.10	3.525e+00	6.298e-03
2.20	0.10	3.755e+00	6.246e-03
2.30	0.10	3.985e+00	6.192e-03

Table 16. Id and Ig vs. Vds (Vgs stepped) for e125 EHFET Simulation at 125C (page 2).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.40	0.10	4.216e+00	6.140e-03
2.50	0.10	4.447e+00	6.087e-03
0.00	0.20	-5.824e-02	1.165e-01
0.10	0.20	3.592e+00	6.405e-02
0.20	0.20	5.796e+00	5.151e-02
0.30	0.20	6.925e+00	4.824e-02
0.40	0.20	7.558e+00	4.714e-02
0.50	0.20	7.981e+00	4.660e-02
0.60	0.20	8.309e+00	4.623e-02
0.70	0.20	8.589e+00	4.592e-02
0.80	0.20	8.844e+00	4.565e-02
0.90	0.20	9.084e+00	4.539e-02
1.00	0.20	9.314e+00	4.514e-02
1.10	0.20	9.539e+00	4.490e-02
1.20	0.20	9.760e+00	4.467e-02
1.30	0.20	9.978e+00	4.444e-02
1.40	0.20	1.019e+01	4.422e-02
1.50	0.20	1.041e+01	4.399e-02
1.60	0.20	1.062e+01	4.377e-02
1.70	0.20	1.083e+01	4.355e-02
1.80	0.20	1.105e+01	4.333e-02
1.90	0.20	1.126e+01	4.312e-02
2.00	0.20	1.147e+01	4.290e-02
2.10	0.20	1.168e+01	4.269e-02
2.20	0.20	1.189e+01	4.248e-02
2.30	0.20	1.210e+01	4.226e-02
2.40	0.20	1.231e+01	4.205e-02
2.50	0.20	1.252e+01	4.184e-02
0.00	0.30	-3.108e-01	6.216e-01
0.10	0.30	8.151e+00	3.313e-01
0.20	0.30	1.373e+01	2.458e-01
0.30	0.30	1.667e+01	2.193e-01
0.40	0.30	1.817e+01	2.099e-01
0.50	0.30	1.902e+01	2.056e-01
0.60	0.30	1.958e+01	2.030e-01
0.70	0.30	1.999e+01	2.011e-01
0.80	0.30	2.033e+01	1.996e-01
0.90	0.30	2.062e+01	1.984e-01
1.00	0.30	2.089e+01	1.972e-01
1.10	0.30	2.114e+01	1.962e-01
1.20	0.30	2.138e+01	1.951e-01
1.30	0.30	2.161e+01	1.942e-01
1.40	0.30	2.184e+01	1.932e-01
1.50	0.30	2.206e+01	1.923e-01
1.60	0.30	2.227e+01	1.914e-01
1.70	0.30	2.249e+01	1.905e-01
1.80	0.30	2.271e+01	1.896e-01
1.90	0.30	2.292e+01	1.887e-01
2.00	0.30	2.313e+01	1.878e-01
2.10	0.30	2.334e+01	1.869e-01

Table 16. Id and Ig vs. Vds (Vgs stepped) for e125 EHFET Simulation at 125C (page 3).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.20	0.30	2.355e+01	1.861e-01
2.30	0.30	2.376e+01	1.852e-01
2.40	0.30	2.397e+01	1.844e-01
2.50	0.30	2.418e+01	1.836e-01
0.00	0.40	-1.537e+00	3.073e+00
0.10	0.40	1.182e+01	1.615e+00
0.20	0.40	2.122e+01	1.105e+00
0.30	0.40	2.659e+01	9.268e-01
0.40	0.40	2.934e+01	8.606e-01
0.50	0.40	3.081e+01	8.314e-01
0.60	0.40	3.169e+01	8.156e-01
0.70	0.40	3.229e+01	8.054e-01
0.80	0.40	3.273e+01	7.979e-01
0.90	0.40	3.309e+01	7.919e-01
1.00	0.40	3.341e+01	7.867e-01
1.10	0.40	3.369e+01	7.821e-01
1.20	0.40	3.395e+01	7.778e-01
1.30	0.40	3.419e+01	7.738e-01
1.40	0.40	3.443e+01	7.699e-01
1.50	0.40	3.466e+01	7.662e-01
1.60	0.40	3.488e+01	7.626e-01
1.70	0.40	3.510e+01	7.591e-01
1.80	0.40	3.532e+01	7.557e-01
1.90	0.40	3.554e+01	7.523e-01
2.00	0.40	3.575e+01	7.489e-01
2.10	0.40	3.596e+01	7.456e-01
2.20	0.40	3.617e+01	7.423e-01
2.30	0.40	3.638e+01	7.390e-01
2.40	0.40	3.659e+01	7.358e-01
2.50	0.40	3.680e+01	7.326e-01
0.00	0.50	-6.276e+00	1.255e+01
0.10	0.50	1.326e+01	7.048e+00
0.20	0.50	2.742e+01	4.621e+00
0.30	0.50	3.615e+01	3.639e+00
0.40	0.50	4.079e+01	3.253e+00
0.50	0.50	4.320e+01	3.088e+00
0.60	0.50	4.455e+01	3.005e+00
0.70	0.50	4.540e+01	2.955e+00
0.80	0.50	4.600e+01	2.921e+00
0.90	0.50	4.645e+01	2.895e+00
1.00	0.50	4.682e+01	2.874e+00
1.10	0.50	4.715e+01	2.856e+00
1.20	0.50	4.743e+01	2.840e+00
1.30	0.50	4.770e+01	2.826e+00
1.40	0.50	4.795e+01	2.812e+00
1.50	0.50	4.819e+01	2.799e+00
1.60	0.50	4.842e+01	2.786e+00
1.70	0.50	4.865e+01	2.774e+00
1.80	0.50	4.887e+01	2.762e+00
1.90	0.50	4.909e+01	2.750e+00

Table 16. Id and Ig vs. Vds (Vgs stepped) for e125 EHFET Simulation at 125C (page 4).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.00	0.50	4.930e+01	2.739e+00
2.10	0.50	4.952e+01	2.727e+00
2.20	0.50	4.973e+01	2.716e+00
2.30	0.50	4.994e+01	2.705e+00
2.40	0.50	5.014e+01	2.694e+00
2.50	0.50	5.035e+01	2.683e+00
0.00	0.60	-1.782e+01	3.565e+01
0.10	0.60	8.840e+00	2.328e+01
0.20	0.60	2.930e+01	1.595e+01
0.30	0.60	4.301e+01	1.222e+01
0.40	0.60	5.079e+01	1.056e+01
0.50	0.60	5.483e+01	9.836e+00
0.60	0.60	5.700e+01	9.487e+00
0.70	0.60	5.828e+01	9.293e+00
0.80	0.60	5.911e+01	9.168e+00
0.90	0.60	5.972e+01	9.080e+00
1.00	0.60	6.019e+01	9.012e+00
1.10	0.60	6.058e+01	8.955e+00
1.20	0.60	6.091e+01	8.907e+00
1.30	0.60	6.122e+01	8.863e+00
1.40	0.60	6.150e+01	8.823e+00
1.50	0.60	6.176e+01	8.786e+00
1.60	0.60	6.201e+01	8.750e+00
1.70	0.60	6.226e+01	8.716e+00
1.80	0.60	6.249e+01	8.682e+00
1.90	0.60	6.272e+01	8.650e+00
2.00	0.60	6.295e+01	8.618e+00
2.10	0.60	6.317e+01	8.587e+00
2.20	0.60	6.339e+01	8.556e+00
2.30	0.60	6.361e+01	8.525e+00
2.40	0.60	6.383e+01	8.495e+00
2.50	0.60	6.404e+01	8.465e+00
0.00	0.70	-3.586e+01	7.172e+01
0.10	0.70	-3.261e+00	5.350e+01
0.20	0.70	2.351e+01	4.018e+01
0.30	0.70	4.301e+01	3.179e+01
0.40	0.70	5.499e+01	2.735e+01
0.50	0.70	6.139e+01	2.527e+01
0.60	0.70	6.472e+01	2.429e+01
0.70	0.70	6.659e+01	2.377e+01
0.80	0.70	6.776e+01	2.345e+01
0.90	0.70	6.855e+01	2.324e+01
1.00	0.70	6.915e+01	2.308e+01
1.10	0.70	6.963e+01	2.295e+01
1.20	0.70	7.003e+01	2.284e+01
1.30	0.70	7.039e+01	2.275e+01
1.40	0.70	7.071e+01	2.267e+01
1.50	0.70	7.101e+01	2.259e+01
1.60	0.70	7.129e+01	2.251e+01
1.70	0.70	7.156e+01	2.244e+01

Table 16. Id and Ig vs. Vds (Vgs stepped) for c125 EHFET Simulation at 125C (page 5).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
1.80	0.70	7.182e+01	2.237e+01
1.90	0.70	7.208e+01	2.231e+01
2.00	0.70	7.233e+01	2.224e+01
2.10	0.70	7.257e+01	2.218e+01
2.20	0.70	7.281e+01	2.212e+01
2.30	0.70	7.305e+01	2.205e+01
2.40	0.70	7.328e+01	2.199e+01
2.50	0.70	7.352e+01	2.193e+01
0.00	0.80	-5.799e+01	1.160e+02
0.10	0.80	-2.110e+01	9.406e+01
0.20	0.80	1.105e+01	7.601e+01
0.30	0.80	3.649e+01	6.273e+01
0.40	0.80	5.370e+01	5.449e+01
0.50	0.80	6.340e+01	5.026e+01
0.60	0.80	6.837e+01	4.825e+01
0.70	0.80	7.101e+01	4.725e+01
0.80	0.80	7.256e+01	4.667e+01
0.90	0.80	7.358e+01	4.630e+01
1.00	0.80	7.431e+01	4.603e+01
1.10	0.80	7.487e+01	4.582e+01
1.20	0.80	7.534e+01	4.566e+01
1.30	0.80	7.574e+01	4.551e+01
1.40	0.80	7.609e+01	4.538e+01
1.50	0.80	7.642e+01	4.526e+01
1.60	0.80	7.673e+01	4.515e+01
1.70	0.80	7.702e+01	4.505e+01
1.80	0.80	7.729e+01	4.495e+01
1.90	0.80	7.756e+01	4.485e+01
2.00	0.80	7.783e+01	4.476e+01
2.10	0.80	7.808e+01	4.466e+01
2.20	0.80	7.834e+01	4.457e+01
2.30	0.80	7.859e+01	4.448e+01
2.40	0.80	7.884e+01	4.439e+01
2.50	0.80	7.908e+01	4.431e+01
0.00	0.90	-8.254e+01	1.651e+02
0.10	0.90	-4.259e+01	1.408e+02
0.20	0.90	-6.309e+00	1.195e+02
0.30	0.90	2.447e+01	1.022e+02
0.40	0.90	4.752e+01	8.978e+01
0.50	0.90	6.181e+01	8.255e+01
0.60	0.90	6.929e+01	7.900e+01
0.70	0.90	7.308e+01	7.730e+01
0.80	0.90	7.516e+01	7.639e+01
0.90	0.90	7.645e+01	7.584e+01
1.00	0.90	7.734e+01	7.546e+01
1.10	0.90	7.799e+01	7.518e+01
1.20	0.90	7.852e+01	7.496e+01
1.30	0.90	7.896e+01	7.477e+01
1.40	0.90	7.935e+01	7.460e+01
1.50	0.90	7.970e+01	7.446e+01

Table 16. Id and Ig vs. Vds (Vgs stepped) for e125 EHFET Simulation at 125C (page 6).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
1.60	0.90	8.002e+01	7.432e+01
1.70	0.90	8.033e+01	7.419e+01
1.80	0.90	8.062e+01	7.407e+01
1.90	0.90	8.090e+01	7.395e+01
2.00	0.90	8.117e+01	7.383e+01
2.10	0.90	8.144e+01	7.372e+01
2.20	0.90	8.170e+01	7.361e+01
2.30	0.90	8.196e+01	7.350e+01
2.40	0.90	8.221e+01	7.339e+01
2.50	0.90	8.247e+01	7.329e+01
0.00	1.00	-1.086e+02	2.171e+02
0.10	1.00	-6.639e+01	1.914e+02
0.20	1.00	-2.704e+01	1.679e+02
0.30	1.00	8.037e+00	1.474e+02
0.40	1.00	3.667e+01	1.312e+02
0.50	1.00	5.661e+01	1.203e+02
0.60	1.00	6.790e+01	1.144e+02
0.70	1.00	7.353e+01	1.116e+02
0.80	1.00	7.643e+01	1.102e+02
0.90	1.00	7.810e+01	1.095e+02
1.00	1.00	7.918e+01	1.090e+02
1.10	1.00	7.996e+01	1.086e+02
1.20	1.00	8.055e+01	1.083e+02
1.30	1.00	8.104e+01	1.081e+02
1.40	1.00	8.146e+01	1.079e+02
1.50	1.00	8.184e+01	1.077e+02
1.60	1.00	8.218e+01	1.076e+02
1.70	1.00	8.250e+01	1.074e+02
1.80	1.00	8.280e+01	1.073e+02
1.90	1.00	8.309e+01	1.072e+02
2.00	1.00	8.337e+01	1.070e+02
2.10	1.00	8.364e+01	1.069e+02
2.20	1.00	8.391e+01	1.068e+02
2.30	1.00	8.418e+01	1.067e+02
2.40	1.00	8.443e+01	1.065e+02
2.50	1.00	8.469e+01	1.064e+02

Table 17. Id and Ig vs. Vgs (Vds stepped) for e125 EHFET Simulation at 125C.

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
0.20	-1.00	2.219e-03	-4.408e-03
0.20	-0.90	2.222e-03	-4.407e-03
0.20	-0.80	2.227e-03	-4.406e-03
0.20	-0.70	2.233e-03	-4.406e-03
0.20	-0.60	2.242e-03	-4.405e-03
0.20	-0.50	2.256e-03	-4.404e-03
0.20	-0.40	2.279e-03	-4.401e-03
0.20	-0.30	2.322e-03	-4.388e-03
0.20	-0.20	2.409e-03	-4.320e-03
0.20	-0.10	2.632e-03	-3.968e-03
0.20	0.00	3.527e-03	-2.121e-03
0.20	0.10	1.947e-02	7.561e-03
0.20	0.20	5.796e+00	5.151e-02
0.20	0.30	1.373e+01	2.458e-01
0.20	0.40	2.122e+01	1.105e+00
0.20	0.50	2.742e+01	4.621e+00
0.20	0.60	2.930e+01	1.595e+01
0.20	0.70	2.351e+01	4.018e+01
0.20	0.80	1.105e+01	7.601e+01
0.20	0.90	-6.309e+00	1.195e+02
0.20	1.00	-2.704e+01	1.679e+02
0.40	-1.00	2.343e-03	-4.409e-03
0.40	-0.90	2.374e-03	-4.408e-03
0.40	-0.80	2.415e-03	-4.407e-03
0.40	-0.70	2.473e-03	-4.406e-03
0.40	-0.60	2.558e-03	-4.406e-03
0.40	-0.50	2.689e-03	-4.405e-03
0.40	-0.40	2.906e-03	-4.402e-03
0.40	-0.30	3.298e-03	-4.389e-03
0.40	-0.20	4.114e-03	-4.324e-03
0.40	-0.10	6.239e-03	-3.983e-03
0.40	0.00	1.480e-02	-2.199e-03
0.40	0.10	1.359e-01	7.128e-03
0.40	0.20	7.558e+00	4.714e-02
0.40	0.30	1.817e+01	2.099e-01
0.40	0.40	2.934e+01	8.606e-01
0.40	0.50	4.079e+01	3.253e+00
0.40	0.60	5.079e+01	1.056e+01
0.40	0.70	5.499e+01	2.735e+01
0.40	0.80	5.370e+01	5.449e+01
0.40	0.90	4.752e+01	8.978e+01
0.40	1.00	3.667e+01	1.312e+02
0.60	-1.00	2.710e-03	-4.409e-03
0.60	-0.90	2.821e-03	-4.409e-03
0.60	-0.80	2.972e-03	-4.408e-03
0.60	-0.70	3.184e-03	-4.407e-03
0.60	-0.60	3.495e-03	-4.406e-03
0.60	-0.50	3.972e-03	-4.405e-03
0.60	-0.40	4.759e-03	-4.402e-03
0.60	-0.30	6.183e-03	-4.390e-03

Table 17. Id and Ig vs. Vgs (Vds stepped) for e125 EHFET Simulation at 125C (page 2).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
0.60	-0.20	9.134e-03	-4.324e-03
0.60	-0.10	1.677e-02	-3.984e-03
0.60	0.00	4.678e-02	-2.204e-03
0.60	0.10	3.770e-01	7.053e-03
0.60	0.20	8.309e+00	4.623e-02
0.60	0.30	1.958e+01	2.030e-01
0.60	0.40	3.169e+01	8.156e-01
0.60	0.50	4.455e+01	3.005e+00
0.60	0.60	5.700e+01	9.487e+00
0.60	0.70	6.472e+01	2.429e+01
0.60	0.80	6.837e+01	4.825e+01
0.60	0.90	6.929e+01	7.900e+01
0.60	1.00	6.790e+01	1.144e+02
0.80	-1.00	3.466e-03	-4.410e-03
0.80	-0.90	3.745e-03	-4.409e-03
0.80	-0.80	4.123e-03	-4.409e-03
0.80	-0.70	4.654e-03	-4.408e-03
0.80	-0.60	5.429e-03	-4.407e-03
0.80	-0.50	6.622e-03	-4.406e-03
0.80	-0.40	8.584e-03	-4.403e-03
0.80	-0.30	1.212e-02	-4.390e-03
0.80	-0.20	1.943e-02	-4.325e-03
0.80	-0.10	3.814e-02	-3.985e-03
0.80	0.00	1.091e-01	-2.208e-03
0.80	0.10	7.087e-01	6.971e-03
0.80	0.20	8.844e+00	4.565e-02
0.80	0.30	2.033e+01	1.996e-01
0.80	0.40	3.273e+01	7.979e-01
0.80	0.50	4.600e+01	2.921e+00
0.80	0.60	5.911e+01	9.169e+00
0.80	0.70	6.775e+01	2.345e+01
0.80	0.80	7.256e+01	4.667e+01
0.80	0.90	7.516e+01	7.639e+01
0.80	1.00	7.642e+01	1.102e+02
1.00	-1.00	4.772e-03	-4.411e-03
1.00	-0.90	5.339e-03	-4.410e-03
1.00	-0.80	6.108e-03	-4.409e-03
1.00	-0.70	7.187e-03	-4.409e-03
1.00	-0.60	8.762e-03	-4.408e-03
1.00	-0.50	1.118e-02	-4.407e-03
1.00	-0.40	1.515e-02	-4.404e-03
1.00	-0.30	2.230e-02	-4.391e-03
1.00	-0.20	3.698e-02	-4.326e-03
1.00	-0.10	7.405e-02	-3.986e-03
1.00	0.00	2.086e-01	-2.213e-03
1.00	0.10	1.094e+00	6.876e-03
1.00	0.20	9.314e+00	4.514e-02
1.00	0.30	2.089e+01	1.972e-01
1.00	0.40	3.341e+01	7.867e-01
1.00	0.50	4.682e+01	2.874e+00

Table 17. Id and Ig vs. Vgs (Vds stepped) for c125 EHFET Simulation at 125C (page 3).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
1.00	0.60	6.019e+01	9.012e+00
1.00	0.70	6.915e+01	2.308e+01
1.00	0.80	7.431e+01	4.603e+01
1.00	0.90	7.733e+01	7.546e+01
1.00	1.00	7.916e+01	1.090e+02
1.20	-1.00	6.791e-03	-4.411e-03
1.20	-0.90	7.802e-03	-4.411e-03
1.20	-0.80	9.175e-03	-4.410e-03
1.20	-0.70	1.110e-02	-4.409e-03
1.20	-0.60	1.391e-02	-4.409e-03
1.20	-0.50	1.821e-02	-4.408e-03
1.20	-0.40	2.527e-02	-4.405e-03
1.20	-0.30	3.791e-02	-4.392e-03
1.20	-0.20	6.370e-02	-4.327e-03
1.20	-0.10	1.278e-01	-3.988e-03
1.20	0.00	3.484e-01	-2.220e-03
1.20	0.10	1.510e+00	6.775e-03
1.20	0.20	9.760e+00	4.467e-02
1.20	0.30	2.138e+01	1.951e-01
1.20	0.40	3.395e+01	7.778e-01
1.20	0.50	4.743e+01	2.840e+00
1.20	0.60	6.091e+01	8.907e+00
1.20	0.70	7.003e+01	2.284e+01
1.20	0.80	7.534e+01	4.566e+01
1.20	0.90	7.849e+01	7.497e+01
1.20	1.00	8.053e+01	1.083e+02
1.40	-1.00	9.692e-03	-4.412e-03
1.40	-0.90	1.134e-02	-4.411e-03
1.40	-0.80	1.358e-02	-4.411e-03
1.40	-0.70	1.672e-02	-4.410e-03
1.40	-0.60	2.128e-02	-4.409e-03
1.40	-0.50	2.828e-02	-4.408e-03
1.40	-0.40	3.971e-02	-4.405e-03
1.40	-0.30	6.012e-02	-4.392e-03
1.40	-0.20	1.014e-01	-4.327e-03
1.40	-0.10	2.019e-01	-3.989e-03
1.40	0.00	5.289e-01	-2.230e-03
1.40	0.10	1.944e+00	6.671e-03
1.40	0.20	1.019e+01	4.422e-02
1.40	0.30	2.184e+01	1.932e-01
1.40	0.40	3.443e+01	7.699e-01
1.40	0.50	4.795e+01	2.812e+00
1.40	0.60	6.150e+01	8.823e+00
1.40	0.70	7.071e+01	2.267e+01
1.40	0.80	7.609e+01	4.538e+01
1.40	0.90	7.932e+01	7.462e+01
1.40	1.00	8.144e+01	1.079e+02
1.60	-1.00	1.365e-02	-4.413e-03
1.60	-0.90	1.617e-02	-4.412e-03
1.60	-0.80	1.959e-02	-4.411e-03

Table 17. Id and Ig vs. Vgs (Vds stepped) for c125 EHFET Simulation at 125C (page 4).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
1.60	-0.70	2.436e-02	-4.411e-03
1.60	-0.60	3.132e-02	-4.410e-03
1.60	-0.50	4.195e-02	-4.409e-03
1.60	-0.40	5.927e-02	-4.406e-03
1.60	-0.30	9.003e-02	-4.393e-03
1.60	-0.20	1.516e-01	-4.328e-03
1.60	-0.10	2.984e-01	-3.991e-03
1.60	0.00	7.480e-01	-2.241e-03
1.60	0.10	2.389e+00	6.565e-03
1.60	0.20	1.062e+01	4.377e-02
1.60	0.30	2.227e+01	1.914e-01
1.60	0.40	3.488e+01	7.626e-01
1.60	0.50	4.842e+01	2.786e+00
1.60	0.60	6.201e+01	8.750e+00
1.60	0.70	7.129e+01	2.251e+01
1.60	0.80	7.672e+01	4.515e+01
1.60	0.90	7.999e+01	7.433e+01
1.60	1.00	8.216e+01	1.076e+02
1.80	-1.00	1.884e-02	-4.414e-03
1.80	-0.90	2.250e-02	-4.413e-03
1.80	-0.80	2.745e-02	-4.412e-03
1.80	-0.70	3.437e-02	-4.411e-03
1.80	-0.60	4.443e-02	-4.411e-03
1.80	-0.50	5.978e-02	-4.410e-03
1.80	-0.40	8.470e-02	-4.407e-03
1.80	-0.30	1.287e-01	-4.394e-03
1.80	-0.20	2.158e-01	-4.329e-03
1.80	-0.10	4.186e-01	-3.992e-03
1.80	0.00	1.002e+00	-2.253e-03
1.80	0.10	2.840e+00	6.458e-03
1.80	0.20	1.105e+01	4.333e-02
1.80	0.30	2.271e+01	1.896e-01
1.80	0.40	3.532e+01	7.557e-01
1.80	0.50	4.887e+01	2.762e+00
1.80	0.60	6.249e+01	8.682e+00
1.80	0.70	7.182e+01	2.237e+01
1.80	0.80	7.729e+01	4.495e+01
1.80	0.90	8.059e+01	7.408e+01
1.80	1.00	8.278e+01	1.073e+02
2.00	-1.00	2.544e-02	-4.414e-03
2.00	-0.90	3.054e-02	-4.414e-03
2.00	-0.80	3.744e-02	-4.413e-03
2.00	-0.70	4.708e-02	-4.412e-03
2.00	-0.60	6.105e-02	-4.411e-03
2.00	-0.50	8.232e-02	-4.410e-03
2.00	-0.40	1.167e-01	-4.408e-03
2.00	-0.30	1.771e-01	-4.395e-03
2.00	-0.20	2.951e-01	-4.330e-03
2.00	-0.10	5.629e-01	-3.994e-03
2.00	0.00	1.287e+00	-2.267e-03

Table 17. Id and Ig vs. Vgs (Vds stepped) for e125 EHFET Simulation at 125C (page 5).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.00	0.10	3.296e+00	6.352e-03
2.00	0.20	1.147e+01	4.290e-02
2.00	0.30	2.313e+01	1.878e-01
2.00	0.40	3.575e+01	7.489e-01
2.00	0.50	4.930e+01	2.739e+00
2.00	0.60	6.295e+01	8.618e+00
2.00	0.70	7.233e+01	2.224e+01
2.00	0.80	7.783e+01	4.476e+01
2.00	0.90	8.114e+01	7.385e+01
2.00	1.00	8.335e+01	1.070e+02
2.20	-1.00	3.364e-02	-4.415e-03
2.20	-0.90	4.052e-02	-4.414e-03
2.20	-0.80	4.983e-02	-4.414e-03
2.20	-0.70	6.280e-02	-4.413e-03
2.20	-0.60	8.159e-02	-4.412e-03
2.20	-0.50	1.101e-01	-4.411e-03
2.20	-0.40	1.560e-01	-4.408e-03
2.20	-0.30	2.360e-01	-4.395e-03
2.20	-0.20	3.905e-01	-4.331e-03
2.20	-0.10	7.314e-01	-3.997e-03
2.20	0.00	1.599e+00	-2.282e-03
2.20	0.10	3.755e+00	6.246e-03
2.20	0.20	1.189e+01	4.248e-02
2.20	0.30	2.355e+01	1.861e-01
2.20	0.40	3.617e+01	7.423e-01
2.20	0.50	4.973e+01	2.716e+00
2.20	0.60	6.339e+01	8.556e+00
2.20	0.70	7.281e+01	2.212e+01
2.20	0.80	7.834e+01	4.457e+01
2.20	0.90	8.167e+01	7.362e+01
2.20	1.00	8.389e+01	1.068e+02
2.40	-1.00	4.360e-02	-4.416e-03
2.40	-0.90	5.265e-02	-4.415e-03
2.40	-0.80	6.486e-02	-4.414e-03
2.40	-0.70	8.187e-02	-4.414e-03
2.40	-0.60	1.064e-01	-4.413e-03
2.40	-0.50	1.436e-01	-4.412e-03
2.40	-0.40	2.033e-01	-4.409e-03
2.40	-0.30	3.063e-01	-4.396e-03
2.40	-0.20	5.024e-01	-4.332e-03
2.40	-0.10	9.234e-01	-3.999e-03
2.40	0.00	1.934e+00	-2.298e-03
2.40	0.10	4.216e+00	6.140e-03
2.40	0.20	1.231e+01	4.205e-02
2.40	0.30	2.397e+01	1.844e-01
2.40	0.40	3.659e+01	7.358e-01
2.40	0.50	5.014e+01	2.694e+00
2.40	0.60	6.383e+01	8.495e+00
2.40	0.70	7.328e+01	2.199e+01
2.40	0.80	7.883e+01	4.439e+01

Table 17. Id and Ig vs. Vgs (Vds stepped) for e125 EHFET Simulation at 125C (page 6).

Vds (V)	Vgs (V)	Id ($\mu\text{A}/\mu\text{m}$)	Ig ($\mu\text{A}/\mu\text{m}$)
2.40	0.90	8.218e+01	7.341e+01
2.40	1.00	8.441e+01	1.065e+02

Table 18. I_g vs. V_{gs} ($V_{ds} = 0$) for e125 EHFET Simulation at 125C.

V_{gs} (V)	I_g ($\mu A/\mu m$)
0.00	-2.623e-10
0.02	1.730e-03
0.04	4.141e-03
0.06	7.499e-03
0.08	1.218e-02
0.10	1.869e-02
0.12	2.776e-02
0.14	4.039e-02
0.16	5.797e-02
0.18	8.244e-02
0.20	1.165e-01
0.22	1.638e-01
0.24	2.295e-01
0.26	3.207e-01
0.28	4.470e-01
0.30	6.216e-01
0.32	8.621e-01
0.34	1.192e+00
0.36	1.643e+00
0.38	2.254e+00
0.40	3.073e+00
0.42	4.161e+00
0.44	5.584e+00
0.46	7.412e+00
0.48	9.714e+00
0.50	1.255e+01
0.52	1.597e+01
0.54	1.999e+01
0.56	2.462e+01
0.58	2.985e+01
0.60	3.565e+01
0.62	4.198e+01
0.64	4.879e+01
0.66	5.605e+01
0.68	6.370e+01
0.70	7.172e+01
0.72	8.005e+01
0.74	8.868e+01
0.76	9.756e+01
0.78	1.067e+02
0.80	1.160e+02
0.82	1.255e+02
0.84	1.352e+02
0.86	1.450e+02
0.88	1.550e+02
0.90	1.651e+02
0.92	1.753e+02
0.94	1.856e+02
0.96	1.960e+02
0.98	2.065e+02

Table 18. I_g vs. V_{ds} ($V_{ds} = 0$) for e125 EHFET Simulation at 125C (page 2).

V_{gs} (V)	I_g ($\mu A/\mu m$)
1.00	2.171e+02
1.02	2.278e+02
1.04	2.385e+02
1.06	2.493e+02
1.08	2.602e+02
1.10	2.711e+02
1.12	2.821e+02
1.14	2.931e+02
1.16	3.042e+02
1.18	3.153e+02
1.20	3.265e+02
1.22	3.377e+02
1.24	3.489e+02
1.26	3.602e+02
1.28	3.715e+02
1.30	3.828e+02
1.32	3.942e+02
1.34	4.056e+02
1.36	4.170e+02
1.38	4.285e+02
1.40	4.400e+02
1.42	4.515e+02
1.44	4.630e+02
1.46	4.745e+02
1.48	4.861e+02
1.50	4.977e+02
1.52	5.093e+02
1.54	5.209e+02
1.56	5.325e+02
1.58	5.442e+02
1.60	5.559e+02

Table 19. Cgd and Cgs vs. Vds (Vgs stepped) for e125 EHFET Simulation at 125C.

Vds (V)	Vgs (V)	Cgd (fF/ μ m)	Cgs (fF/ μ m)
0.00	-1.00	2.861e-01	5.050e-01
0.50	-1.00	2.861e-01	5.050e-01
1.00	-1.00	2.861e-01	5.050e-01
1.50	-1.00	2.861e-01	5.050e-01
2.00	-1.00	2.861e-01	5.050e-01
2.50	-1.00	2.861e-01	5.050e-01
0.00	-0.75	2.861e-01	5.845e-01
0.50	-0.75	2.861e-01	5.845e-01
1.00	-0.75	2.861e-01	5.845e-01
1.50	-0.75	2.861e-01	5.845e-01
2.00	-0.75	2.861e-01	5.845e-01
2.50	-0.75	2.861e-01	5.845e-01
0.00	-0.50	2.861e-01	6.964e-01
0.50	-0.50	2.861e-01	6.964e-01
1.00	-0.50	2.861e-01	6.964e-01
1.50	-0.50	2.861e-01	6.964e-01
2.00	-0.50	2.861e-01	6.964e-01
2.50	-0.50	2.861e-01	6.964e-01
0.00	-0.25	2.861e-01	8.639e-01
0.50	-0.25	2.861e-01	8.639e-01
1.00	-0.25	2.861e-01	8.639e-01
1.50	-0.25	2.861e-01	8.639e-01
2.00	-0.25	2.861e-01	8.639e-01
2.50	-0.25	2.861e-01	8.639e-01
0.00	0.00	2.861e-01	1.137e+00
0.50	0.00	2.861e-01	1.137e+00
1.00	0.00	2.861e-01	1.137e+00
1.50	0.00	2.861e-01	1.137e+00
2.00	0.00	2.861e-01	1.137e+00
2.50	0.00	2.861e-01	1.137e+00
0.00	0.25	2.861e-01	1.646e+00
0.50	0.25	2.861e-01	1.646e+00
1.00	0.25	2.861e-01	1.646e+00
1.50	0.25	2.861e-01	1.646e+00
2.00	0.25	2.861e-01	1.646e+00
2.50	0.25	2.861e-01	1.646e+00
0.00	0.50	2.861e-01	2.858e+00
0.50	0.50	2.861e-01	2.858e+00
1.00	0.50	2.861e-01	2.858e+00
1.50	0.50	2.861e-01	2.858e+00
2.00	0.50	2.861e-01	2.858e+00
2.50	0.50	2.861e-01	2.858e+00
0.00	0.75	2.861e-01	8.067e+00
0.50	0.75	2.861e-01	8.067e+00
1.00	0.75	2.861e-01	8.067e+00
1.50	0.75	2.861e-01	8.067e+00
2.00	0.75	2.861e-01	8.067e+00
2.50	0.75	2.861e-01	8.067e+00

Table 20. Cgd and Cgs vs. Vgs (Vds stepped) for e125 EHFET Simulation at 125C.

Vds (V)	Vgs (V)	Cgd (fF/ μ m)	Cgs (fF/ μ m)
0.00	-1.00	2.861e-01	5.050e-01
0.00	-0.90	2.861e-01	5.338e-01
0.00	-0.80	2.861e-01	5.665e-01
0.00	-0.70	2.861e-01	6.037e-01
0.00	-0.60	2.861e-01	6.466e-01
0.00	-0.50	2.861e-01	6.964e-01
0.00	-0.40	2.861e-01	7.548e-01
0.00	-0.30	2.861e-01	8.241e-01
0.00	-0.20	2.861e-01	9.076e-01
0.00	-0.10	2.861e-01	1.010e+00
0.00	0.00	2.861e-01	1.137e+00
0.00	0.10	2.861e-01	1.299e+00
0.00	0.20	2.861e-01	1.513e+00
0.00	0.30	2.861e-01	1.804e+00
0.00	0.40	2.861e-01	2.220e+00
0.00	0.50	2.861e-01	2.858e+00
0.00	0.60	2.861e-01	3.932e+00
0.00	0.70	2.861e-01	6.051e+00
0.00	0.80	2.861e-01	1.074e+01
0.00	0.90	2.861e-01	1.386e+01
0.00	1.00	2.861e-01	1.426e+01
2.50	-1.00	2.861e-01	5.050e-01
2.50	-0.90	2.861e-01	5.338e-01
2.50	-0.80	2.861e-01	5.665e-01
2.50	-0.70	2.861e-01	6.037e-01
2.50	-0.60	2.861e-01	6.466e-01
2.50	-0.50	2.861e-01	6.964e-01
2.50	-0.40	2.861e-01	7.548e-01
2.50	-0.30	2.861e-01	8.241e-01
2.50	-0.20	2.861e-01	9.076e-01
2.50	-0.10	2.861e-01	1.010e+00
2.50	0.00	2.861e-01	1.137e+00
2.50	0.10	2.861e-01	1.299e+00
2.50	0.20	2.861e-01	1.513e+00
2.50	0.30	2.861e-01	1.804e+00
2.50	0.40	2.861e-01	2.220e+00
2.50	0.50	2.861e-01	2.858e+00
2.50	0.60	2.861e-01	3.932e+00
2.50	0.70	2.861e-01	6.051e+00
2.50	0.80	2.861e-01	1.074e+01
2.50	0.90	2.861e-01	1.386e+01
2.50	1.00	2.861e-01	1.426e+01

Table 21. Ig vs. Vgs for ed25 Diode Simulation at 25C.

Vgs (V)	Ig ($\mu\text{A}/\mu\text{m}$)
0.00	-2.040e-13
0.02	2.165e-06
0.04	5.674e-06
0.06	1.137e-05
0.08	2.062e-05
0.10	3.566e-05
0.12	6.011e-05
0.14	9.986e-05
0.16	1.645e-04
0.18	2.697e-04
0.20	4.407e-04
0.22	7.189e-04
0.24	1.171e-03
0.26	1.907e-03
0.28	3.105e-03
0.30	5.052e-03
0.32	8.219e-03
0.34	1.337e-02
0.36	2.174e-02
0.38	3.535e-02
0.40	5.746e-02
0.42	9.336e-02
0.44	1.516e-01
0.46	2.458e-01
0.48	3.977e-01
0.50	6.416e-01
0.52	1.030e+00
0.54	1.641e+00
0.56	2.585e+00
0.58	4.008e+00
0.60	6.077e+00
0.62	8.964e+00
0.64	1.280e+01
0.66	1.766e+01
0.68	2.354e+01
0.70	3.038e+01
0.72	3.807e+01
0.74	4.652e+01
0.76	5.561e+01
0.78	6.525e+01
0.80	7.536e+01
0.82	8.586e+01
0.84	9.671e+01
0.86	1.078e+02
0.88	1.192e+02
0.90	1.309e+02
0.92	1.427e+02
0.94	1.546e+02
0.96	1.668e+02
0.98	1.790e+02

Table 21. Ig vs. Vds for ed25 Diode Simulation at 25C (page 2).

Vgs (V)	Ig ($\mu\text{A}/\mu\text{m}$)
1.00	1.914e+02
1.02	2.039e+02
1.04	2.165e+02
1.06	2.292e+02
1.08	2.419e+02
1.10	2.548e+02
1.12	2.677e+02
1.14	2.806e+02
1.16	2.936e+02
1.18	3.067e+02
1.20	3.198e+02
1.22	3.330e+02
1.24	3.462e+02
1.26	3.595e+02
1.28	3.728e+02
1.30	3.861e+02
1.32	3.994e+02
1.34	4.128e+02
1.36	4.262e+02
1.38	4.397e+02
1.40	4.531e+02
1.42	4.666e+02
1.44	4.801e+02
1.46	4.937e+02
1.48	5.072e+02
1.50	5.208e+02
1.52	5.344e+02
1.54	5.480e+02
1.56	5.617e+02
1.58	5.753e+02
1.60	5.890e+02

Table 22. C vs. Vgs for ed25 Diode Simulation at 25C.

Vgs (V)	C (fF/ μm)
-1.00	8.856e-01
-0.95	9.163e-01
-0.90	9.489e-01
-0.85	9.837e-01
-0.80	1.021e+00
-0.75	1.060e+00
-0.70	1.103e+00
-0.65	1.148e+00
-0.60	1.197e+00
-0.55	1.249e+00
-0.50	1.306e+00
-0.45	1.368e+00
-0.40	1.434e+00
-0.35	1.507e+00
-0.30	1.587e+00
-0.25	1.674e+00
-0.20	1.770e+00
-0.15	1.876e+00
-0.10	1.994e+00
-0.05	2.126e+00
0.00	2.274e+00
0.05	2.441e+00
0.10	2.631e+00
0.15	2.849e+00
0.20	3.100e+00
0.25	3.393e+00
0.30	3.738e+00
0.35	4.148e+00
0.40	4.636e+00
0.45	5.202e+00
0.50	5.785e+00
0.55	6.114e+00
0.60	5.607e+00
0.65	4.122e+00
0.70	2.586e+00
0.75	1.580e+00
0.80	1.009e+00
0.85	6.826e-01
0.90	4.873e-01
0.95	3.636e-01
1.00	2.812e-01

Table 23. Ig vs. Vgs for ed125 Diode Simulation at 125C.

Vgs (V)	Ig ($\mu\text{A}/\mu\text{m}$)
0.00	-2.853e-16
0.02	2.584e-04
0.04	6.554e-04
0.06	1.265e-03
0.08	2.203e-03
0.10	3.643e-03
0.12	5.856e-03
0.14	9.256e-03
0.16	1.448e-02
0.18	2.250e-02
0.20	3.483e-02
0.22	5.375e-02
0.24	8.280e-02
0.26	1.274e-01
0.28	1.957e-01
0.30	3.003e-01
0.32	4.602e-01
0.34	7.039e-01
0.36	1.074e+00
0.38	1.631e+00
0.40	2.464e+00
0.42	3.691e+00
0.44	5.468e+00
0.46	7.978e+00
0.48	1.142e+01
0.50	1.597e+01
0.52	2.177e+01
0.54	2.889e+01
0.56	3.731e+01
0.58	4.696e+01
0.60	5.775e+01
0.62	6.956e+01
0.64	8.225e+01
0.66	9.571e+01
0.68	1.098e+02
0.70	1.246e+02
0.72	1.398e+02
0.74	1.555e+02
0.76	1.715e+02
0.78	1.879e+02
0.80	2.046e+02
0.82	2.215e+02
0.84	2.387e+02
0.86	2.561e+02
0.88	2.737e+02
0.90	2.915e+02
0.92	3.094e+02
0.94	3.275e+02
0.96	3.456e+02
0.98	3.640e+02

Table 23. Ig vs. Vds for ed125 Diode Simulation at 125C (page 2).

Vgs (V)	Ig ($\mu\text{A}/\mu\text{m}$)
1.00	3.824e+02
1.02	4.009e+02
1.04	4.195e+02
1.06	4.382e+02
1.08	4.570e+02
1.10	4.758e+02
1.12	4.947e+02
1.14	5.137e+02
1.16	5.328e+02
1.18	5.519e+02
1.20	5.710e+02
1.22	5.902e+02
1.24	6.095e+02
1.26	6.288e+02
1.28	6.481e+02
1.30	6.675e+02
1.32	6.869e+02
1.34	7.064e+02
1.36	7.259e+02
1.38	7.454e+02
1.40	7.650e+02
1.42	7.846e+02
1.44	8.042e+02
1.46	8.238e+02
1.48	8.435e+02
1.50	8.632e+02
1.52	8.829e+02
1.54	9.026e+02
1.56	9.224e+02
1.58	9.422e+02
1.60	9.620e+02

Table 24. C vs. Vgs for ed125 Diode Simulation at 125C.

Vgs (V)	C (fF/ μ m)
-1.00	8.856e-01
-0.95	9.163e-01
-0.90	9.489e-01
-0.85	9.837e-01
-0.80	1.021e+00
-0.75	1.060e+00
-0.70	1.103e+00
-0.65	1.148e+00
-0.60	1.197e+00
-0.55	1.249e+00
-0.50	1.306e+00
-0.45	1.368e+00
-0.40	1.434e+00
-0.35	1.507e+00
-0.30	1.587e+00
-0.25	1.674e+00
-0.20	1.770e+00
-0.15	1.876e+00
-0.10	1.994e+00
-0.05	2.126e+00
0.00	2.274e+00
0.05	2.441e+00
0.10	2.630e+00
0.15	2.847e+00
0.20	3.095e+00
0.25	3.378e+00
0.30	3.691e+00
0.35	4.001e+00
0.40	4.191e+00
0.45	4.015e+00
0.50	3.277e+00
0.55	2.266e+00
0.60	1.444e+00
0.65	9.228e-01
0.70	6.140e-01
0.75	4.285e-01
0.80	3.124e-01
0.85	2.364e-01
0.90	1.845e-01
0.95	1.477e-01
1.00	1.209e-01

PROCESS CONTROL MONITOR

This section of the manual contains the design and documentation of the Process Control Monitor (PCM). It is composed of two modules, each 1 by 2mm. The modules contain structures for circuit analysis, device modeling, and device process/metal interconnect testing.

The PCM modules can be provided by AT&T along with the layout design rule file to reside in a users CAD system. They can be converted to GDSII or any other format that is in use. It is required that at least 20 of each module be included on a wafer for statistical data base analysis. The user must also orient the PCM modules, such that, all HFET gates on the wafer are in the same direction.

PCM MODULE 1

Module 1 contains digital circuit analysis and model correlation structures. The module contains SFFL and DCFL inverters and gates to extract AC and DC noise margins, power dissipation, and propagation delay. It also contains HFET devices to extract ADVICE or SPICE model parameters. The placement of modeling and logic circuits on the same module permits the extraction of model parameters and the direct correlation between simulated and measured circuit responses. This will enhance the modeling effort and improve the circuit performance assurance of the foundry.

Module 1 contains the following structures:

EHFETs used in model parameter extraction and correlation

L = 1 μ m, W = 10 μ m EHFET.

L = 1 μ m, W = 4 μ m DHFET.

L = 1 μ m, W = 50 μ m (2 x 25) EHFET.

L = 1 μ m, W = 50 μ m (2 x 25) DHFET.

Open calibration pads.

7 stage D-flip flop ring oscillator to extract flip flop propagation delay from the data, clear, and preset inputs to output.

31 stage DCFL inverter ring oscillator.

31 stage SFFL inverter ring oscillator.

31 stage SFFL 3-input NOR gate ring oscillator, one input driven to extract worst case high state AC noise margin.

31 stage SFFL 3-input NOR gate ring oscillator, all inputs driven to extract worst case low state AC noise margin.

31 stage 2-input NAND gate ring oscillator.

Input/Output buffer test circuit.

The DC transfer curves and DC noise margins of the logic gates are extracted from the following circuits.

DCFL inverter.

SFFL inverter.

SFFL 2-input NAND gate.

SFFL 5-input NOR gate to extract DC transfer curve and noise margins versus fan-in.

PCM MODULE 2

Module 2 contains the HFET characterization test structures. This module contains EHFETs, DHFETs, and schottky diodes from which DC I/V, capacitance, and ADVICE or SPICE model parameters can be extracted. The module also contains S-parameter testers to extract device capacitances and S-parameters. It will also be used in performing FMA on the HFET structures. A wide range of HFET and schottky diode device widths are included to check for device scaling versus width.

Module 2 contains the following structures:

The HFET S-parameter measurement is done on the following structures:

$L = 1\mu\text{m}$, $W = 50\mu\text{m}$ (1 x 50) EHFET and DHFET.

$L = 1\mu\text{m}$, $W = 50\mu\text{m}$ (2 x 25) EHFET and DHFET.

$L = 1\mu\text{m}$, $W = 50\mu\text{m}$ (4 x 12.5) EHFET and DHFET.

$L = 2\mu\text{m}$, $W = 25\mu\text{m}$ EHFET Diode and DHFET Diode.

Open calibration pads for each of the above structures.

The following HFET devices are used for DC current/voltage and capacitance/voltage measurement. The devices are also used for ADVICE and SPICE model parameter extraction.

$L = 1\mu\text{m}$, $W = 2, 3, 6, 12, 18$, and $25\mu\text{m}$ EHFETs and DHFETs.

$L = 2\mu\text{m}$, $W = 6\mu\text{m}$ EHFETs and DHFETs.

$L = 1\mu\text{m}$, $W = 18\mu\text{m}$ Dual Gate EHFET.

$L = 2\mu\text{m}$, $W = 2, 3, 6$, and $12\mu\text{m}$ EHFET Diodes.

$L = 2\mu\text{m}$, $W = 3, 6$, and $12\mu\text{m}$ DHFET Diodes.

$L = 1\mu\text{m}$, $W = 2\mu\text{m}$ DHFET cascode structure.

Open calibration pads.

PCM MODULE 3

Module 3 contains the device process and interconnect test structures. This module is the in process test module for the SARGIC/HFET process. The structures in module 3 are used to extract SARGIC/HFET process parameters, as well as, isolation and backgating effects. The device structure test permits extracting sheet resistances of N/N+ implants, contact resistance, isolation, and backgating effects. The interconnect tester permits extracting metal sheet resistance, metal line width and spacing, via contact resistance, and metal to metal leakage currents caused by metal spiking through the dielectric.

Module 3 test structures:

The sheet resistance of N+ implants and ohmic contact resistance are measured using the following structures:

DHFET/N+ transmission line structure.
N(DHFET)/N+ van der pauws, 1 square resistor.

Device isolation and backgating effects in HFETs are measured as follows:

EHFET devices with minimum spacing.
Source follower backgating test structure.

The split cross bridge structure is used to measure metal sheet resistance and line widths on the following levels:

Gate metal (GMT)
Ohmic metal (OMT)
Bottom metal (BMT)
Top metal (TMT)

A four terminal test structure is used in measuring metal/metal contact resistance and.

Gate/Bottom metal
Ohmic/Bottom metal
Bottom/Top metal
1.0 and 1.5 μ m via1 to via2 continuity tester.

The metal/metal leakage currents caused by metal spikes through the dielectric, dielectric constant, and thickness are measured as follows:

GMT/BMT/TMT comb. structure, with 2/6 μ m lines and spaces.
MIM (Metal Insulator Metal) capacitor.

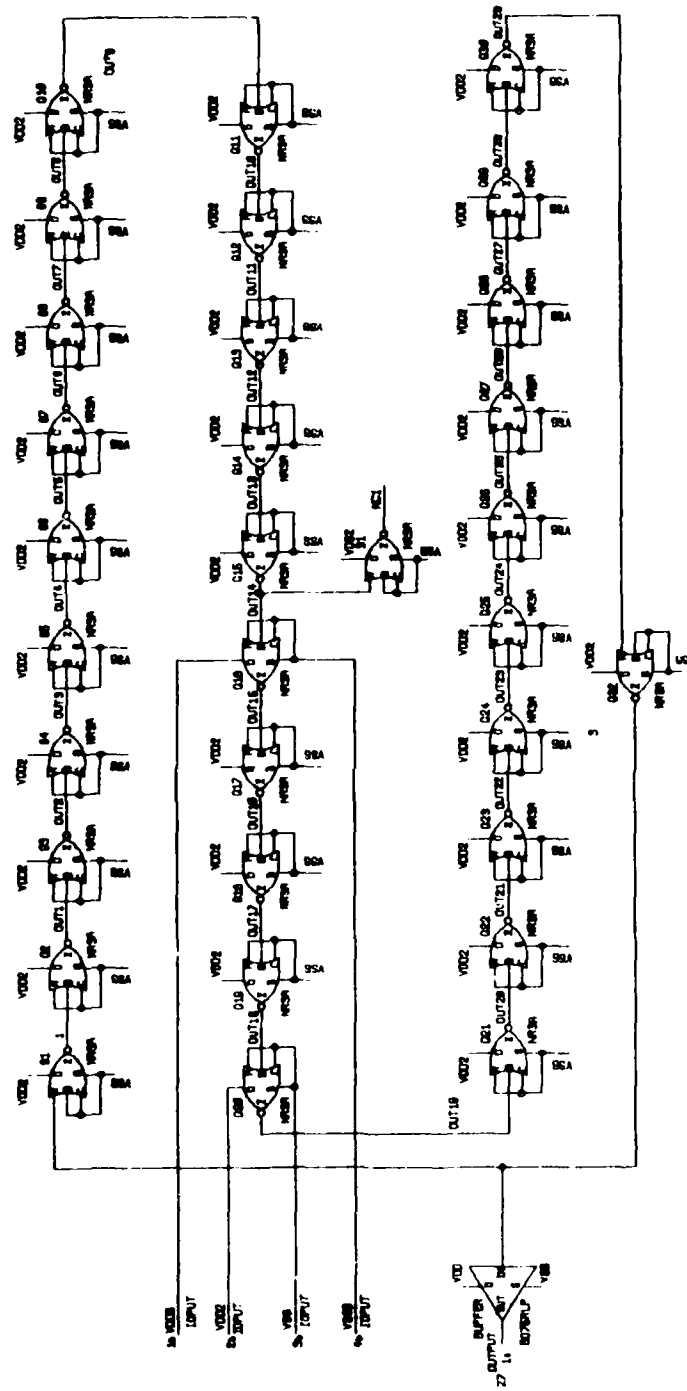
A prometrix structure is also included to measure gate metal line width. Also an EHFET and DHFET of 18 μ m width and a 1 μ m gate length are included for DC I/V measurement.

PROCESS CONTROL MONITOR

LIST OF FIGURES AND TABLES

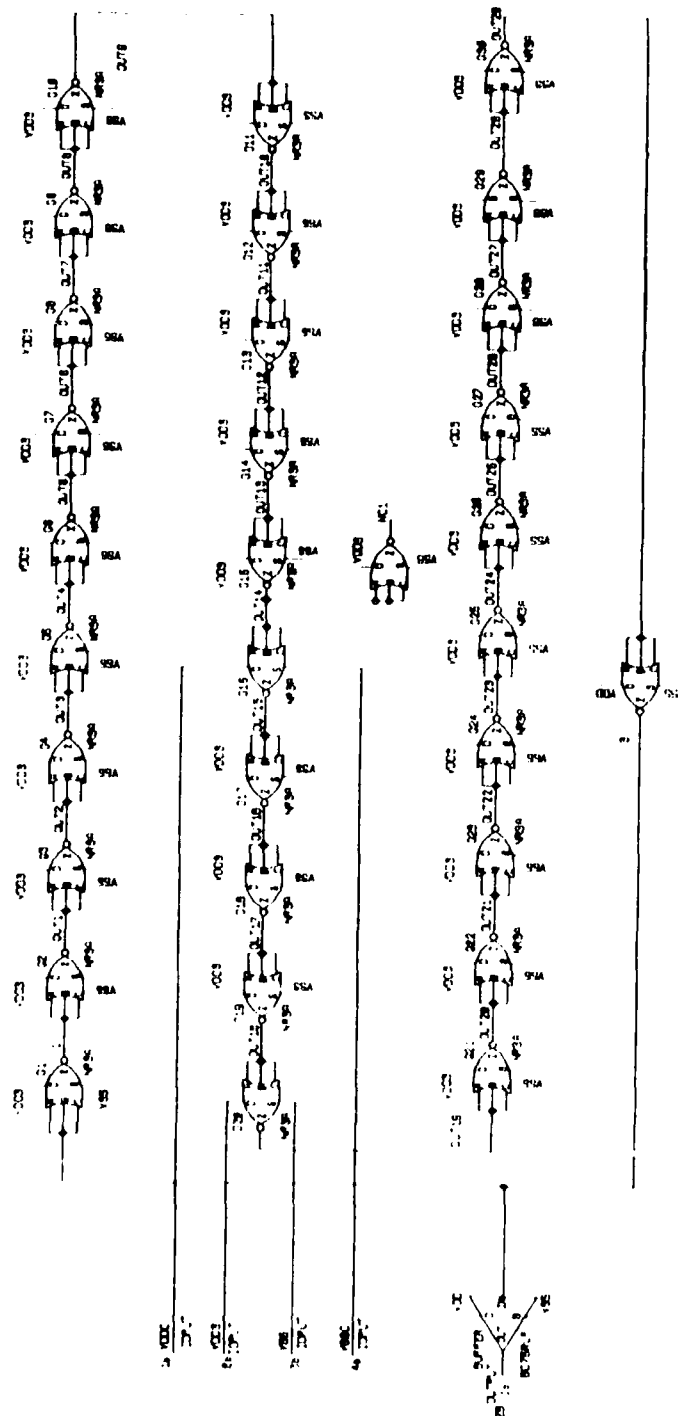
Figure 1.	SFFL Inverter Ring Oscillator Schematic
Figure 2.	3-Input NOR Gate Ring Oscillator Sch. (1 Input driven)
Figure 3.	3-Input NOR Gate Ring Oscillator Sch. (3 Inputs driven)
Figure 4.	2-Input NAND Gate Ring Oscillator Sch.
Figure 5.	DCFL Inverter Ring Oscillator Schematic
Figure 6.	D-Flip Flop Ring Oscillator Schematic
Figure 7.	Loaded DC Logic Gate Tester
Module 1	Layout
Module 2	Layout
Module 3	Layout

SFFL 3-INPUT NOR GATE RING OSCILLATOR SCH. (1 INPUT DRIVES)



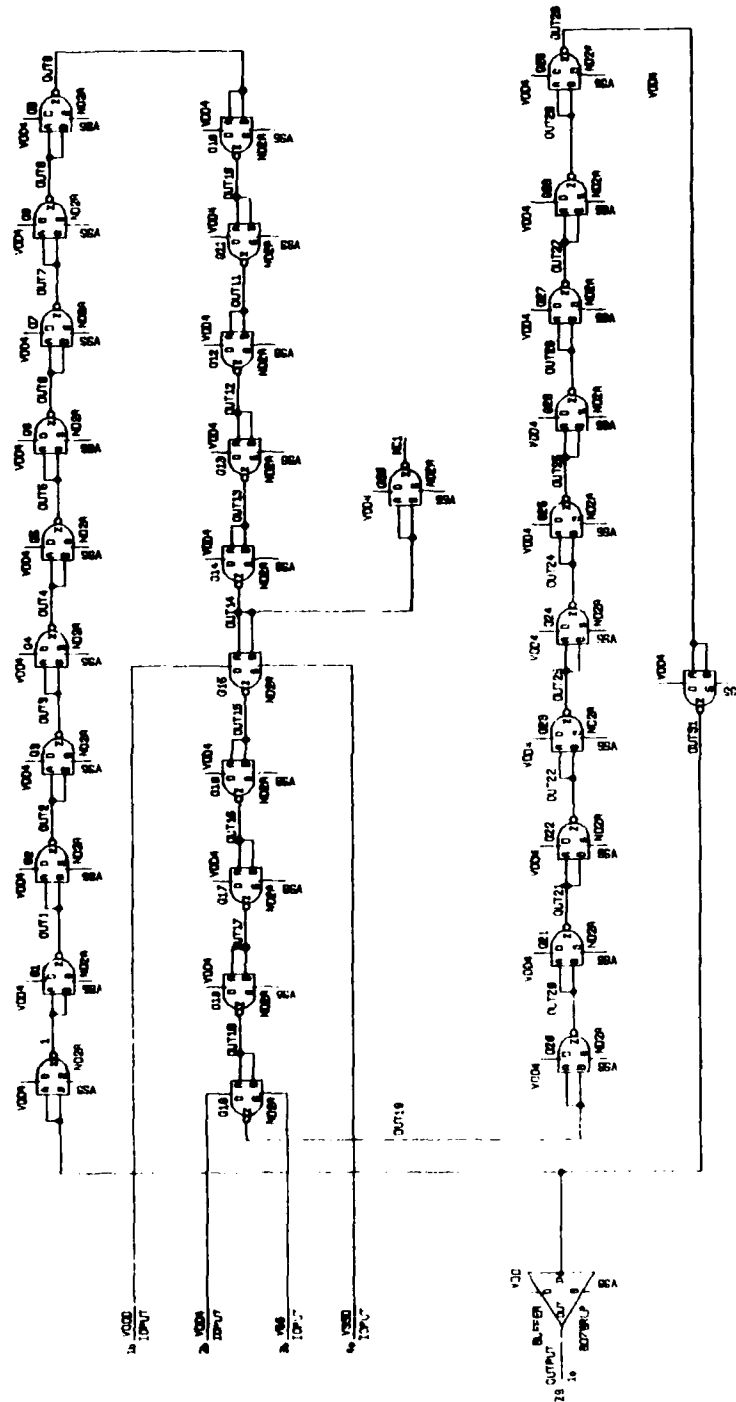
SCHEMATIC PROCESS CONTROL MONITOR	ESCH	ADP	9
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FIGURE 2	DATE	REV	1
	BS	4/11/88	

REV	1	DATE	4/11/68
BY	CS	DESIGN	SS
CHK	SS	DATE	4/11/68
APP	SS	DATE	4/11/68
PROJ	SS	DATE	4/11/68
FIGURE	3		
PROCESS CONTROL MONITOR			



SEE 3-INPUT NOR GATE RING OSCILLATOR SCH. 3 INPUTS DRIVEN

SPFL 2-INPUT NAND GATE RING OSCILLATOR SCH.



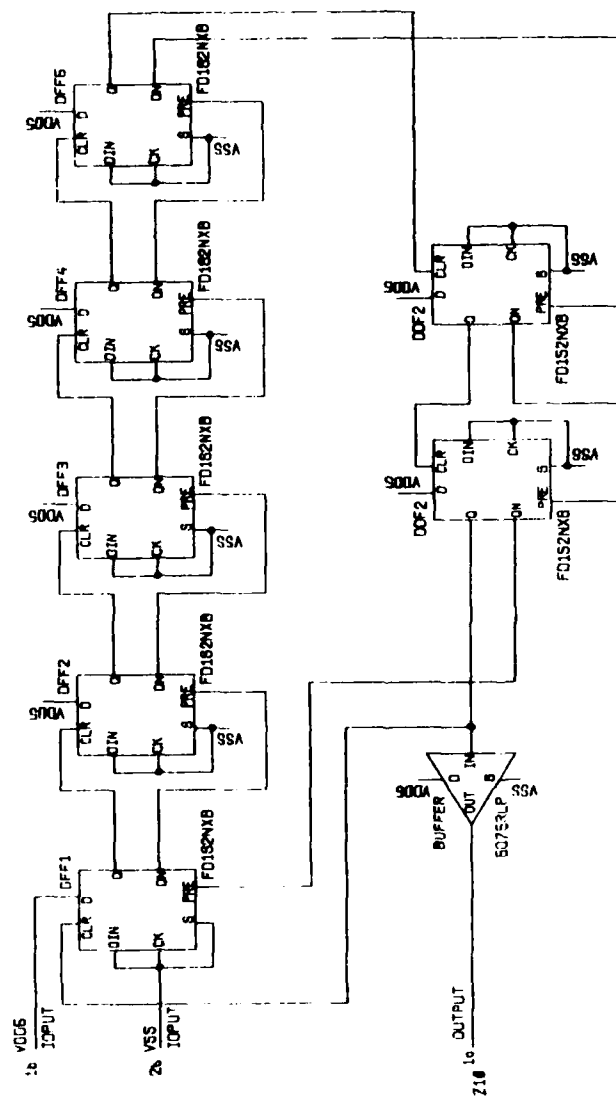
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PROCESS CONTROL MONITOR	DATE: 4/13/88	BY: 6S
FIGURE 4		

6	2	3	4	5	6	7	8	9
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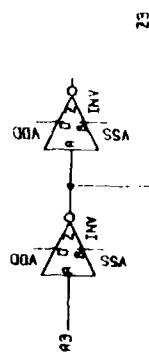
D-FLIP FLOP RING OSCILLATOR SCHEMATIC



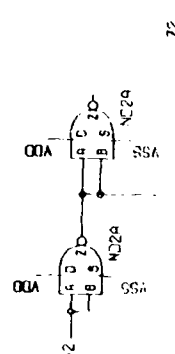
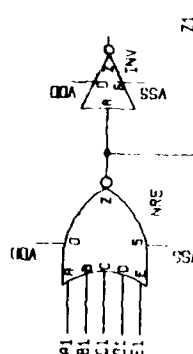
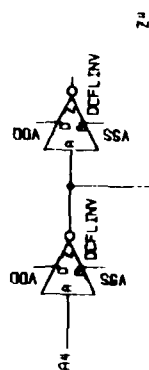
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FIGURE 6		DATE	REV
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LOADED DC LOGIC GATE TESTER

SFTL LOADED GATES



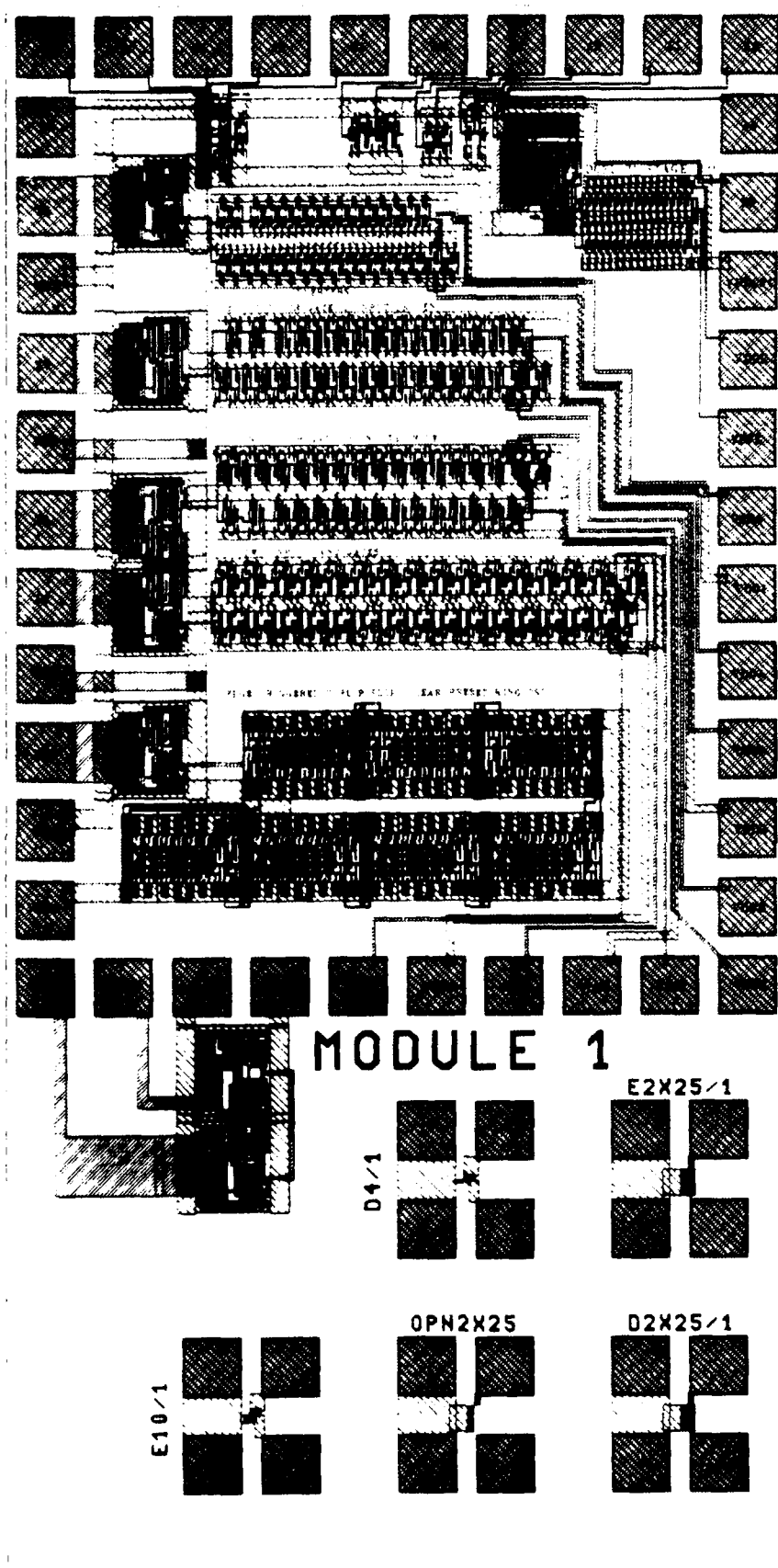
DC TEST



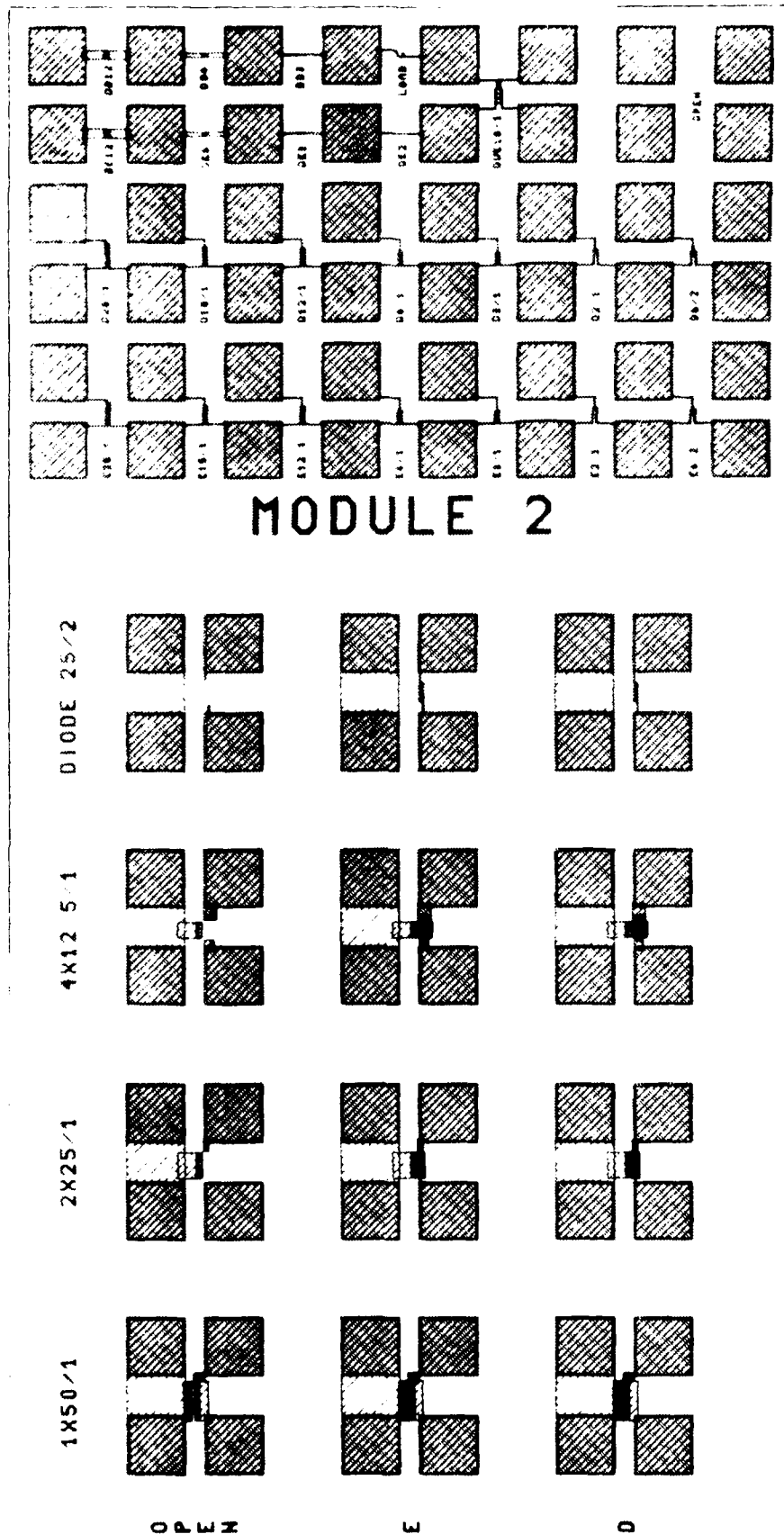
SCHEMATIC
PROCESS CONTROL MONITOR
FIGURE 7

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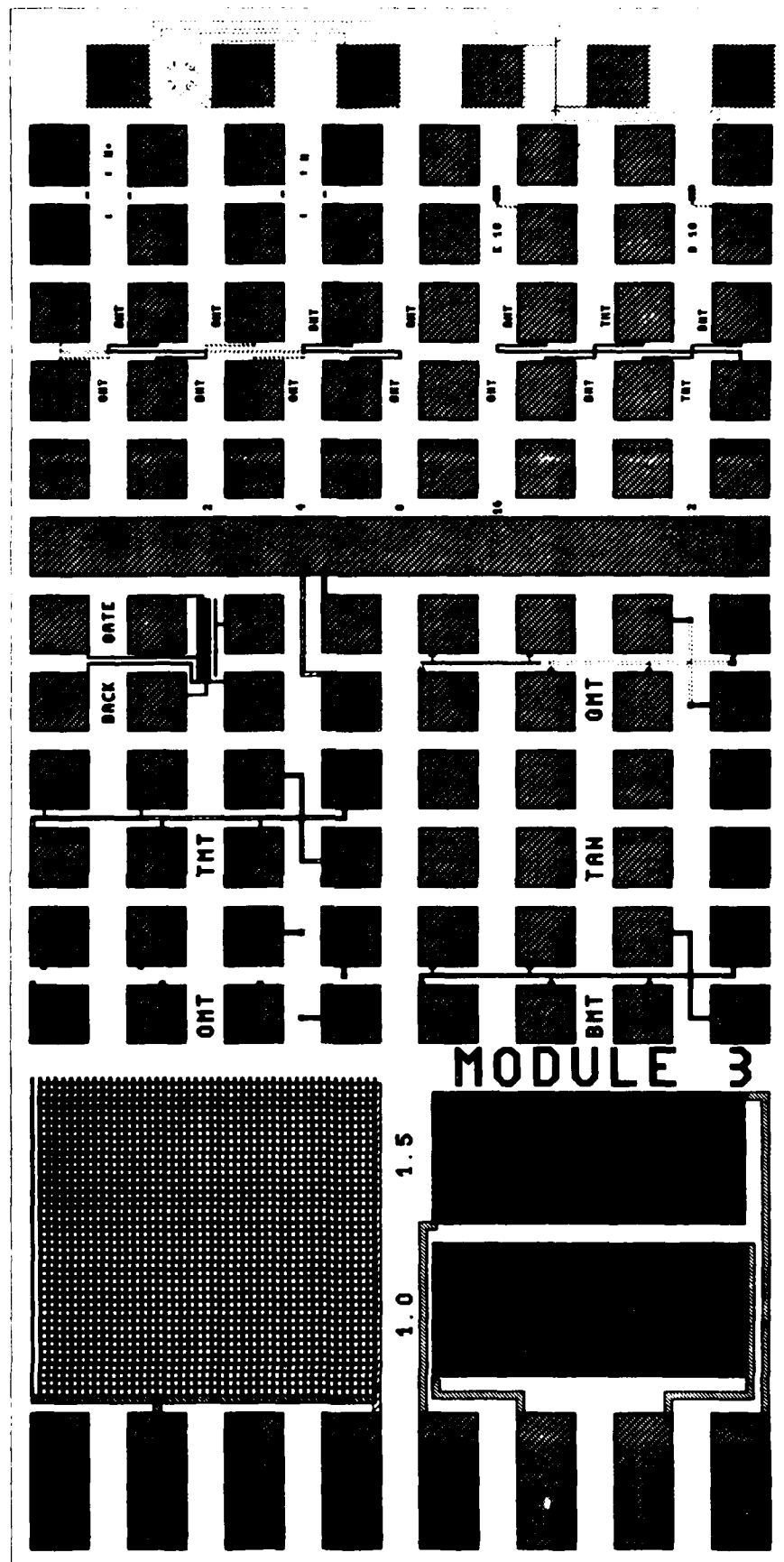
PROCESS CONTROL MONITOR (PCM)



PCM Layout: Module 1.



PCM Layout: Module 2.



PCM Layout: Module 3.

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